



Short Circuit Analysis of Power Distribution Network Including Distributed Generations

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ABSTRACT

The crisis of traditional fuels in the world has become the main reason behind the search on renewable energy resources. Therefore, the researchers become interested with distributed generation (DG) and how to connect them with the main power network to achieve the maximum benefit from these resources. But before connecting these resources with the main grid on the low voltage level, worst case scenario that could occurs must be analyzed first. This paper introduces a procedure to study the effect of the DG units on distribution systems during the short circuit. This effect is measured in terms of fault current and voltage total harmonic distortion. The main objective of this paper is to determine the maximum DG penetration that can be adopted in distribution system without degrading the system performance or change the protection design or coordination. The European technical standard and IEEE-1547 standard are used to compare the results obtained.

General purpose Alternative Transients Program (ATP) version of Electromagnetic Transient Program (EMTP) is used to accomplish the above goals. IEEE 13 node test feeder distribution system is used in this work.

Index Term – Distribution system, Short circuit, Power quality, Harmonics, IEEE 13 node distribution feeder, EMTP/ATP program.

تحليل الخطأ في شبكات التوزيع الكهربية المشتملة علي مصادر توليد موزع

الخلاصة

أصبحت أزمة الوقود التقليدي في العالم هي السبب الرئيسي وراء البحث عن مصادر متجددة للطاقة لذلك اهتم الباحثون بمصادر التوليد الموزع وكيفية ربطها مع شبكة توليد الكهرباء الرئيسية لتحقيق أقصي استفادة من هذه المصادر للكر فبل ربط هذه المصادر مع الشبكة لا بد من دراسة وتحليل أسوأ السيناريو هات التي من الممكن أن تحدث. هذا البحث يقدم طريقة لدراسة تأثير مصادر التوليد الموزع وكيفية السيناريو هات التي من الممكن أن تحدث. هذا البحث يقدم طريقة لدراسة تأثير مصادر للوليد الموزع علي شبكات التوزيع أثناء حدوث الخطأ. هذا الميناريو هات التي من الممكن أن تحدث. هذا البحث يقدم طريقة لدراسة تأثير مصادر التوليد الموزع علي شبكات التوزيع أثناء حدوث الخطأ. هذا التأثير يتم تقديم ما يقد من الممكن أن تحدث. هذا البحث يقدم طريقة لدراسة تأثير مصادر التوليد الموزع علي شبكات التوزيع أثناء حدوث الخطأ. هذا التأثير يتم تقديم عن طريق تعلي أسوأ مع علي شبكات التوزيع أثناء حدوث الخطأ. هذا التأثير يتم تقديم عن من ما ما ما لي التوافقيات الموجودة في موجة الجهد. ان الهدف الرئيسي من هذا البحث هو تحديل أسوأ تقدم عن من ما ما يقد ما قدم طريقة لدراسة تأثير مصادر التوليد الموزع علي شبكات التوزيع أثناء حدوث الخطأ. هذا التأثير يتم تقديم عن من طريق تحليل تيار الخطأ وحساب اجمالي التوافقيات الموجودة في موجة الجهد. ان الهدف الرئيسي من هذا البحث هو تحديد أقصي نسبة مشاركة يم من أن تشارك بها هذه المصادر دون ان تحدث خلل او تغيير في أداء الشبكة أو تؤثر علي تناسق نظام الحماية المصادر مع التخلير التقنية الأوربية والمعايير الأمريكية رقم ١٥-10 لموارنة النتائج التي حصلنا عليها.

استخدم البر نامج الشامل لمحاكاة الظواهر العابرة EMTP-ATP لتحقيق الهدف من الدراسة . كما تم استخدام IEEE 13 node test feeder لتمثيل شبكات توزيع الكهرباء .

Nomenclature

- **DG** Distributed Generation
- **EPS** Electrical Power System
- **PO** Power Quality
- **EMTP** Electromagnetic Transients Program
- **ATP** Alternative Transients Program
- THD_v Voltage Total Harmonic Distortion
- **THD**_C Current Total Harmonic Distortion

1. INTRODUCTION

It is commonly accepted that, the traditional large power plants are now challenged by the DG sources. Now the generation is not exclusive to one level. Hence, some of the energy demand is supplied by the main power grid and another part is produced by the DG. The DG is considered as an electrical source connected to the power system, in a point very close to/or at consumer's site, which is small enough compared with the centralized power plant [1].

The effects of the DG can be classified as environmental, technical and economic effects. So, it has played a very vital role for improving the voltage profiles in Electrical Power Systems (EPS). But, it could have negative impacts such as operating conflicts for fault clearing, reclosing and interference with relaying [2]. The DG could increase the short circuit currents, and reverse the power flow in the distribution network resulting in making it as an active network. While the electrical distribution networks were designed to operate in one direction as a passive network. So, there will be a trade-off between the positive and negative impacts of the DG especially with increasing the penetration levels [3, 4].

On the other hand, the short circuit phenomenon is one of the most important factors causing the transient in EPS. All voltage sources in EPS tend to contribute in the fault during the short circuit. So many researchers were concerning with the impact of the DG on EPS. In [5], the authors proved that regarding short circuit currents,

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induction machines are more favorable than the synchronous ones. And regards to voltage dips, synchronous machines are preferred because during faults they inject a reactive power to the network. While in [6], the author proved that the DG has a positive impact on the characteristics of voltage sags (remaining voltage) caused at any voltage level. And in [7], the authors analyzed the impact of the DG on the location of faults. They proved that, the presence of DG decreased the value of the apparent reactance seen from the main substation. Thus, the estimate locations calculated by using impedance based on fault location methodologies will be closer than the actual location of the fault.

In master thesis [8], the author analyzed the impact of the DG on fault response. He measured the impact of the DG in terms of fault current and the remaining voltage at the source bus only. He didn't include the effect of the DG on the total harmonic distortion (THD) either in current (THD_C) or voltage (THD_V). He presented the DG as a three phase voltage source with constant penetration level.

This paper introduces a procedure to determine the maximum DG penetration levels that can be adopted in distribution system without violating any standard or change the coordination of the distribution system. Another goal is to estimate the worst fault location that can be occurred in order to be prepared for it. The method will be used to assess the above goal is based on, monitoring the current, voltage, and calculating the THD_V either, with the presence of the DG or without it during and after the short circuit condition with various fault locations, and different DG penetration. The results obtained will be compared with the permissible standard.

2. DG CLASSIFICATION

Figure 1 shows the DG classification according to the principles of operation and the interface between the distribution network and the DG.

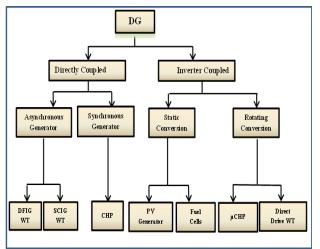


Figure 1: Classification of DG

This classification is important to determine the short circuit contribution of the DG to a disturbance in the distribution network. It is stated that inverter coupled DG hardly contributes to fault current. Hence, PV systems, fuel cells, direct drive WT and the micro CHP do not have to be considered in fault current calculations and the evaluation of the protective system. The directly coupled DG does contribute to the fault current and cannot be neglected in the fault current calculations and protective system studies [9]. In this paper, a synchronous generator is used to represent the DG source.

3. CAUSES OF TRANSIENTS IN POWER SYSTEMS

The main causes of excessive voltages and currents in power systems are lightning, switching, short circuits and resonance conditions. The transient phenomena which follows the short circuit condition are small compared with lightning and switching but yet very severe at times and can lead to shutdown of the system. The short circuit transient phenomena are classified according to the speed of transients under low speed transients [8].

If there is a short circuit in the system, the presence of one or more DG can affect the monitoring of voltages and currents at the substation. The main supply generation will not have to inject as much power to the line because of the DG presence [7].

4. POWER QUALITY OF DISTRIBUTION SYSTEMS

Even the best distribution systems are subject to some changes from time-to-time. These changes affect the power quality (PQ) in terms of harmonics, voltage flicker, voltage sag, voltage swell, grounding and interruption; usually characterize the quality of electric power systems. Usually the term PQ refers to maintaining a sinusoidal waveform of bus voltages at rated voltage and frequency with least amount of interruptions [10, 11].

The large scale deployments of DG_S are expected to deteriorate of PQ [4]. Regarding to the PQ indices, this paper is focused on harmonic analysis to show the impact of the DG on distribution systems.

5. HARMONIC ANALYSIS

The fundamental frequency of the AC electric power distribution system is 50 Hz. *A harmonic frequency* is defined by any sinusoidal frequency, which is a multiple of the fundamental frequency. Harmonic frequencies can be even or odd multiples of the sinusoidal fundamental frequency [11].

5.1 Harmonic Calculation

In most cases, any periodic distorted power system waveform (voltage, current, flux, etc.) can be represented as a series consisting of a dc term and an infinite sum of sinusoidal terms using Fourier analysis as shown in Eq.(1). While in Eq.(2) the total harmonic distortion (THD) is defined.

$$f(t) = F_0 + \sum_{\substack{i=1\\ \sqrt{\sum_{i=1}^{\infty} E^2}}^{\infty} \sqrt{2}F_i \cos(i\omega_0 t + \theta_i)$$
(1)

THD(%) =
$$\frac{\sqrt{\sum_{i=2}^{n} F_i^2}}{F_1} * 100\%$$
 (2)

Where ω_0 is the fundamental power frequency, F_i is the magnitude and θ_i is the phase angle for ith term in the series [12].

The THD has the following properties [13]:

- THD is zero for a perfectly sinusoidal waveform
- As the distortion increases, THD becomes very large
- A commonly used THD level in distribution system is 5%.
- THD of either current or voltage may be calculated.

5.2 Effects of Harmonics on Equipment

There are two major categories of harmonics effects on equipment [10, 13]:

- a) Heating effects in power handling equipment such as conductors, motors, capacitors, and transformers that most often reduced the equipment operating life and caused the skin effect of conductors.
- b) Disruption of operation that includes, for the most part, electronically controlled equipment such as incorrect operation of the control process using zero crossing synchronization.

6. PROPOSED PROCEDURE

The proposed procedure used to determine the maximum penetration of the DG is depending on the value of the fault current and THD_V along the voltage spectrum (one cycle before the fault begins up to return the voltage to its steady state after the fault vanished) at all tested buses. Also, it is estimates the worst fault location depending on the following steps:

- 1. Apply the fault at different locations of the distribution system
- 2. Monitor the current, voltage profile and compute the THD_V during short circuit *without* the DG connection (base case).
- 3. Connect the DG at penetration level start from 10% to 30% of total load demand.
- 4. Apply the same faults at the same locations after connecting the DG
- 5. Compute the short circuit current and the THD_V at every penetration level
- 6. Compare the results obtained "without the DG and every penetration of the DG" with the corresponding value in the standard.
- Evaluate the maximum DG penetration level that the distribution system can adopt without violating the standard such as the European technical standard, IEEE-1547 and IEEE 519 power quality standard.
- 8. Finally, identify the worst fault location that the distribution systems degrading the PQ limit due to the DG connection.

7. TEST SYSTEM

IEEE 13 node test feeder is used in this study with the DG. This system has different voltage levels, 115 kV, 4.16 kV, and 480 V, short and relatively highly loaded

feeder (4.07 MVA). The original configuration of the feeder has a capacity of 5 MVA. The DG capacity is taken as 0.410 MVA.

Also, the feeder has one substation voltage regulator consisting of three single-phase units connected in wye connection. It has overhead and underground lines with variety of phasing, shunt capacitor banks, in-line transformer and unbalanced spot and distributed loads [14]. Table A_1 in appendix shows the synchronous generator parameters used to represent the DG.

Figure 2 shows the fault locations and the DG location on the distribution system. The faults are simulated at bus 645, 633, 692, and 684 to show the impact of the DG on the fault currents at different fault locations.

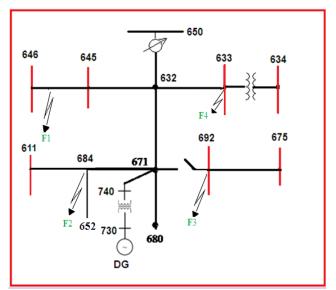


Figure 2: IEEE 13 node with the DG connection at different fault locations

In this paper, ATP-EMTP software is used as a simulation tool [15,16].

8. SIMULATION RESULTS

The proposed procedure which described on section 5 is applied on the test system. The effect of the DG on the system during short circuits is divided to two main factors namely fault current and voltage harmonic content as shown in the following sections.

8.1 Impact of the DG on Fault Current

Apply the fault at every location without connecting the DG (Base Case). Figure 3 shows the fault currents (I_F) versus the fault locations.

It is shown in figure 3 that, the value of I_F at the location 633 is higher than the corresponding values at other locations because, it is the nearest location to the source. And the only factor controlling the fault current is the line impedance of the distribution feeder. As the distance from the source to the fault location increases, the fault current decreases.

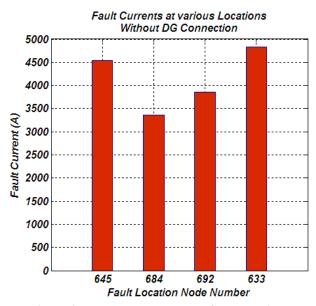


Figure 3: Fault currents versus fault locations

In order to clarify the impact of the DG on the fault currents, the DG is connecting with penetration levels starts from 0 to 30% by step 10%, And recording the obtained results.

Table 1 shows the percentage increase of the fault currents due to DG connection at different penetration levels according to the following equation.

$$\% I_F increase = \frac{I_F \text{ with } DG - I_F \text{ without } DG}{I_F \text{ without } DG} * 100$$

 Table 1:- Percentage increase of fault currents due to DG connection

Fault location			
Penetration	10%	20%	30%
645	8.57	14.94	19.85
684	20.6	37.53	52.29
692	22.25	41.53	58.79
633	9.27	16.04	21.38

It is shown from table 1 that, the increase of I_F has the lowest value at the bus 645 as its location is far from the DG location. On the other hand, when the fault occurred at the bus 692, it has the highest increase in fault current as it is separated from the DG location by a switch only. It is the nearest location to the DG location.

Figure 4 shows the fault current itself versus the fault location with different DG penetration level.

It is shown in figure 4 that, the DG affects the operation of distribution networks by providing bidirectional flows of fault currents. It is making the fault current at location 692 "close to the DG location" at 30 % penetration level, higher than the corresponding value at location 633 which has the highest value without the DG connection. So, Hence the protection coordination may be changed by the presence of DG.

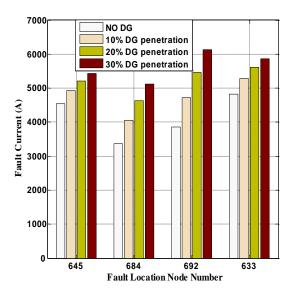


Figure 4: fault current itself versus the fault location at different DG penetration level

It is recommended that 10% DG penetration level is acceptable. Because at 10% DG penetration level, the coordination of the distribution system is the same, and presence of the DG increase the efficiency of the system by increasing the voltage at some customers. Above 10 % penetration level "20 % penetration" the I_F at 692 become higher than corresponding value at location 645, and DG is start affect the coordination.

8.2 Impact of the DG on Voltage Harmonic During Faults

To fully study the effect of the DG source in distribution system during fault on voltage harmonic, a fault started at (0.3 ms) zero crossing point and cleared at (0.34 ms). The faults are represented at four different locations:

- At bus 692 on phase B
- At bus 684 on phase A
- At bus 645 on phase B
- At bus 633 on phase A

For each case, the faulty phase voltage is divided at each one cycle (one cycle before the fault occurred to return the voltage to its steady state values. The THD_V is calculated at each cycle. While changing the DG penetrations are from 10% to 30%.

Case one:- Fault at bus 692

In this case, the fault is occurred at bus 692 which represents the highest I_F variation. The bus 692 is farthest bus from the source bus (2000 *ft.*). Also, it is the nearest location to the DG. The THD_V is calculated at all tested buses such as, bus 740 (DG bus), bus 632 (source bus), bus 675 (near bus to the DG) and bus 634 (low voltage bus).

Figure 5& 6 show the impact of the DG Penetration on THD_V at the bus 632 (source bus) and at the DG location respectively.

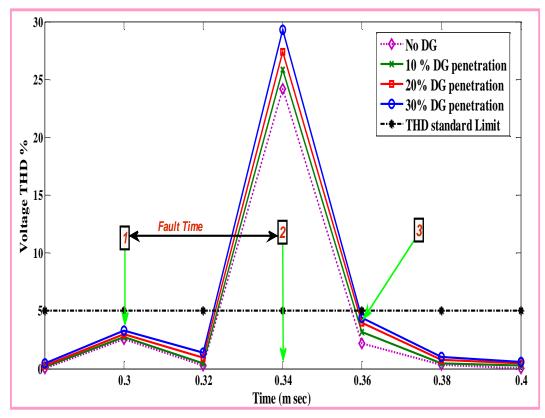


Figure 5: Impact of the DG penetration level on source THD_V

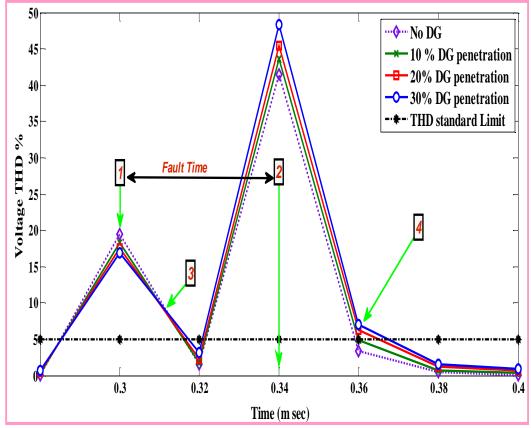


Figure 6: Impact of the DG penetration level at the DG location

It is shown from figure 5 that, presence of the DG increases the THD_V especially with increase the penetration level of the DG. At the beginning of the fault (point 1), the THD_V is increased, but it is in the limit. While, at the fault vanished (point 2), the THD_V is increased by high percentage affected by changing the DG penetration level. If the DG penetration level has reached 30%, THD_V is beyond the permissible limit as shown at point 3.

It is shown from figure 6 that, THD_V at the DG location is outside the limit without the DG connection otherwise at the source location. And increasing the penetration level of the DG decreased the THD_V at the time of the fault occurred (point 1) due to the DG power injection. At the time of the fault vanished (point 2), THD_V increase with penetration level increased.

The main observation from this figure that, presence of the DG with penetration level up to10%, increasing the transient time of the fault as shown at point 4. The THD_V has degrading the acceptable limit and required more than one cycle to return to acceptable value. So, increasing the penetration level of the DG has a negative impact on the transient time when, the fault location is near to the DG location.

Table 2 shows the response of the THD_V at all tested buses along the fault time interval.

Table 2:%THDvsummary at all tested buses when
fault at the bus 692

Time msec. Penetration%	0.28- 0.3	0.3- 0.32	0.32- 0.34	0.34- 0.36	0.36- 0.38	0.38- 0.4		
	1	- Bus (6 32(Sour	ce bus)				
No DG	9e-3	2.54	0.26	24.2	2.19	0.31		
10% DG pen.	0.18	2.76	0.49	25.8	3.18	0.49		
20% DG pen.	0.3	3.01	0.93	27.4	3.98	0.79		
30% DG pen.	0.44	3.28	1.4	29.3	4.42	1.00		
	2- Bus 740 (DG bus)							
No DG	9e-3	19.45	1.56	41.5	3.41	0.47		
10% DG pen.	0.26	18.27	1.73	43.6	4.89	0.75		
20% DG pen.	0.45	17.49	2.28	45.5	<mark>6.27</mark>	1.2		
30% DG pen.	0.66	16.95	3.15	48.4	<mark>7.02</mark>	1.53		
	3- B	us 675(n	earest bu	is to the	DG)			
No DG	9e-3	19.7	1.54	42.2	3.58	0.49		
10% DG pen.	0.26	18.5	1.68	44.6	<mark>5.13</mark>	0.78		
20% DG pen.	0.46	17.6	2.17	46.7	<mark>6.59</mark>	1.24		
30% DG pen.	0.67	17.1	3	49.9	<mark>7.4</mark>	1.57		
4- Bus 634(Low voltage bus)								
No DG	9e-3	2.29	0.26	23.9	2.16	0.3		
10% DG pen.	0.17	2.51	0.49	25.6	3.11	0.49		
20% DG pen.	0.3	2.77	0.94	27.1	3.92	0.78		
30% DG pen.	0.44	3.05	1.41	29	4.37	1		

It is shown from table 2 that, THD_V decrease with increase DG penetration at bus 675(near bus to DG location) and bus 740 (DG location) otherwise the bus(632) and bus 634. The decrease in THD_V return to DG helps to stabilize the voltage at the sudden change.

✤ Case 2:- Fault at the bus 684

Repeating the same procedure, but in this case the fault is applied at the bus 684. This case is similar to the previous case when, the fault is at bus 692. Table 3 shows the THD_V along the fault transient time at all tested buses.

Table 3: %THD_v summary at all tested buses when fault at the bus 684

Time msec. Penetration%	0.28- 0.3	0.3- 0.32	0.32- 0.34	0.34- 0.36	0.36- 0.38	0.38- 0.4	
	1-	Bus 6	32(Sour	ce bus)			
No DG	9e-3	2.93	0.19	20.5	2.27	0.35	
10% DG pen.	0.16	3.2	0.56	21.66	3.03	0.47	
20% DG pen.	0.28	3.48	1.06	22.5	3.68	0.73	
30% DG pen.	0.4	3.75	1.59	23.42	3.71	0.74	
	2- Bus 740 (DG bus)						
No DG	0.009	13.2	0.79	35.14	3.48	0.54	
10% DG pen.	0.24	12.4	1.34	36.23	4.67	0.718	
20% DG pen.	0.42	11.94	2.35	36.94	<mark>5.74</mark>	1.11	
30% DG pen.	0.59	11.68	3.47	38.04	<mark>5.74</mark>	1.11	
	3- E	Bus 675(r	near bus	to the D	G)		
No DG	0.009	13.62	0.79	36	3.72	0.57	
10% DG pen.	0.248	12.69	1.33	37.3	4.99	0.76	
20% DG pen.	0.43	12.15	2.33	38.2	<mark>6.14</mark>	1.17	
30% DG pen.	0.59	11.85	3.45	39.49	<mark>6.17</mark>	1.18	
4- Bus 634(Low voltage bus)							
No DG	9e-3	2.68	0.19	20.16	2.23	0.34	
10% DG pen.	0.16	2.96	0.56	21.3	2.98	0.47	
20% DG pen.	0.28	3.26	1.06	22.14	3.62	0.72	
30% DG pen.	0.39	3.55	1.58	23.0	3.65	0.73	

It is shown from table 3 that, this case is less effect than previous case.

Case 3:- Fault at bus 645

This fault is present the lowest I_F variation. Figure 7 & 8 show the impact of the DG penetration on THD_V at the source bus and the DG location respectively during the fault.

It is shown from figure 7 that, at the fault occur the THD_V is outside the limit 5% without the DG connection, and decrease with increase the penetration level as seen at point 1. At the moment of the fault clear (point 2), the THD_V reach to 26% but, it has decrease to 2.8% in about one cycle as shown at point 4.

It is shown from figure 8 that, the THD_V decreased by 34.86% (16.06% :10.46%) as seen at the point 1. This decrease return to, the fault is far from the DG location.

After the fault, the THD_V increasing with increasing the DG penetration level as displayed at point 3 to reach at 30% penetration to 4.74%. So, it is beyond to degrading the allowable limit.

At the fault clear, the THD_V decreasing with increasing the DG penetration level as displayed at point 2 to reach the THD_V decrease to 4.26% (30.7 % : 29.39%). At This fault location, the THD_V decreased at the moment of fault occur and fault clear otherwise, the THD_V increasing with increasing the DG penetration level as displayed at point 4. After that it has return to acceptable limit in about one cycle.

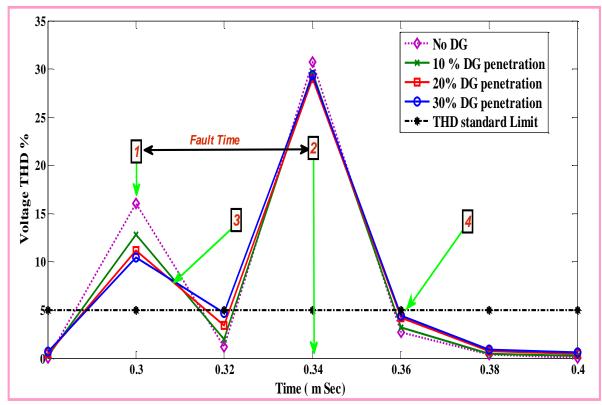


Figure 7: Impact of the DG penetration level on THD_v at source bus

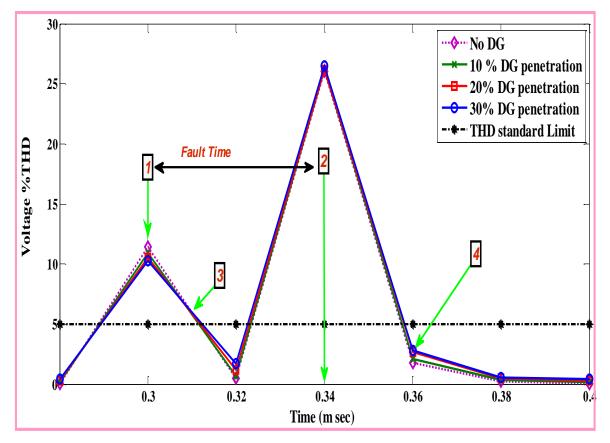


Figure 8: Impact of the DG penetration level on THD_V at the DG location

Table 4 shows the THD_V at all tested buses when the fault is at the bus 645.

Time msec. Penetration%	0.28- 0.3	0.3- 0.32	0.32- 0.34	0.34- 0.36	0.36- 0.38	0.38- 0.4	
	1. Bus 632(Source bus)						
No DG	0.009	11.42	0.46	26.03	1.76	0.24	
10% DG pen.	0.17	10.93	0.7	26.14	2.08	0.33	
20% DG pen.	0.3	10.53	1.22	26.16	2.66	0.48	
30% DG pen.	0.44	10.24	1.73	26.5	2.8	0.56	
	2. Bus 740 (DG bus)						
No DG	0.009	16.06	1.2	30.7	2.7	0.36	
10% DG pen.	0.26	12.8	1.97	29.64	3.2	0.5	
20% DG pen.	0.45	11.19	3.39	29.02	4.18	0.74	
30% DG pen.	0.66	10.46	4.7	29.39	4.42	0.89	
	3. Bu	s 675(ne	arest bu	is to the	DG)		
No DG	0.009	16.67	1.3	31.2	2.9	0.38	
10% DG pen.	0.26	13.37	2	30.29	3.38	0.53	
20% DG pen.	0.46	11.66	3.44	29.79	4.40	0.77	
30% DG pen.	0.67	10.9	4.72	29.31	4.67	0.92	
4. Bus 634(Low voltage bus)							
No DG	0.009	10.98	0.47	25.7	1.75	0.24	
10% DG pen.	0.18	10.53	0.7	25.8	2.07	0.33	
20% DG pen.	0.30	10.1	1.22	25.85	2.63	0.48	
30% DG pen.	0.45	9.9	1.73	26.26	2.77	0.58	

Table 4: %THD_v summary at all tested buses when fault at the bus 645

It is shown in table 4 that, the THD_V at the bus 675 is approximately equal to THD_V at bus 740, and THD_V at bus 634 is approximately equal to THD_V at bus 632.

Case 4 :- Fault at the bus 633

This case is similar to the previous case when the fault at the bus 645. Table 5 summarizes the THD_V values at all tested buses.

Time	0.28-	0.3-	0.32-	0.34-	0.36-	0.38-
msec.	0.3	0.32	0.34	0.36	0.38	0.4
Penetration%						••••
	1-	Bus 6	32(Sourd	e bus)		
No DG	0.009	10.63	0.56	26.81	2.73	0.42
10% DG pen.	0.16	10.31	1	27.05	3.07	0.62
20% DG pen.	0.28	10.08	1.65	27.05	3	0.61
30% DG pen.	0.4	9.95	2.31	27.2	2.21	0.34
2- Bus 740 (DG bus)						
No DG	0.009	15.82	1.3	31.3	4.17	0.63
10% DG pen.	0.24	12.59	2.82	30.19	4.75	0.91
20% DG pen.	0.42	11.36	4.73	29.31	4.59	0.94
30% DG pen.	0.59	11.19	6.43	29.02	3.65	0.57
	3. Bu	s 675(ne	arest bu	is to the	DG)	
No DG	0.009	16.86	1.43	32.16	4.46	0.67
10% DG pen.	0.24	13.4	2.88	31.1	5.08	0.99
20% DG pen.	0.43	12.0	4.78	30.3	4.94	0.95
30% DG pen.	0.6	11.8	6.49	30.2	2.25	0.35
4. Bus 634(Low voltage bus)						
No DG	0.009	17.34	0.9	30.26	2.68	0.418
10% DG pen.	0.16	17.13	1.04	30.72	3	0.62
20% DG pen.	0.28	17	1.3	30.88	2.95	0.6
30% DG pen.	0.4	16.9	1.62	31.13	4.17	0.63

Table 5: %THD_V summary at all tested buseswhen fault at the bus 633

9. CONCLUSIONS

In this paper, the voltage total harmonic distortion is taken as a reference to determine the technical impact of the DG on distribution system during faults. It was a perfect index to determine the maximum penetration level of the DG during the short circuit. The fault is simulated at different location on the distribution system, and the DG located at the far location from the source to improve the voltage of the system. Different DG penetration levels were used from 0 to 30%.

EMTP-ATP simulation tools and IEEE 13 node distribution test feeder were used to achieve the goal of this paper. The fundamental theory associated with harmonics has been used to calculate the voltage total harmonic distortion. Based on the obtained results it can be concluded that:-

- At the moment of the fault occurrence, the THD_V at source location is higher than the acceptable limit (5%) in the case of the fault locations near to the source while it has lower value than 5% in the case of the fault location far from the source bus.
- Increased the penetration level of the DG affected the coordination of the electrical distribution system. Above 10% DG penetration level, coordination of the system may change due to bidirectional power flow, and THD_V crossed the acceptable limit affected by increasing the penetration level of the DG. The worst case scenario, when the DG was near to the fault location.
- When the fault is far from the DG location, the THD_v at the beginning of fault and at the clearing of fault decreased by a percentage from 4.26% to 34.86% which helps to stabilize the voltage at the sudden change.
- When the fault is near to the DG location, the transient time to return the THD_V to its allowable limit after clearing the fault was increased by increasing the DG penetration.

Appendix

Table A1. 410 KVA Synchronous Generator Parameters

1 al ametel S							
V _{Rated} (V)	480	X _d ' (pu)	0.21				
KVA _{Rated}	410	X _q ' (pu)	0.18				
P _{Rated} (KW)	350	X _d " (pu)	0.13				
V Scheduled(pu)	1	X _q " (pu)	0.11				
Q max(pu)	0.5	ra (pu)	0				
Q min(pu)	-0.25	r. (pu)	0				
pf	0.85365	r _{il} (pu)	0				
X _d (pu)	1.76	X _{1r} (pu)	0				
X _q (pu)	1.66	X ₀ (pu)	0.065				

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