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VLSI IMPLEMENTATION OF A FUZZY LOGIC MEMBERSHIP FUNCTION CIRCUIT

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ABSTRACT

In this paper we present the design of an analog membership function circuit for fuzzy logic controllers. The presented circuit has been simulated on PSpice. A VLSI implementation of the circuit has also been performed using the L-EDIT™ program. The resulting layout has then been tested using L-EDIT and the test results coincide with the PSpice™ simulation results.

KEY WORDS

Fuzzy logic control, Membership function, VLSI implementation.

INTRODUCTION

DURING the past several years, fuzzy control has emerged as one of the most active and fruitful areas for research in the application of fuzzy set theory .Fuzzy control has found many applications in the realm of industrial processes , especially those which do not lend themselves to control by conventional methods because of a lack of quantitative data regarding the input-output relations.

Fuzzy control is based on fuzzy logic; a logical system that is much closer in spirit to human thinking and natural language than traditional logical systems. The fuzzy logic controller (FLC), based on fuzzy logic, provides a means of converting a linguistic control strategy based on expert knowledge into an automatic control strategy [1],[2]. The basic configuration of an FLC, shown in Fig. (1), consists of three main components that are used to reach a crisp solution to a specific problem [3],[4].

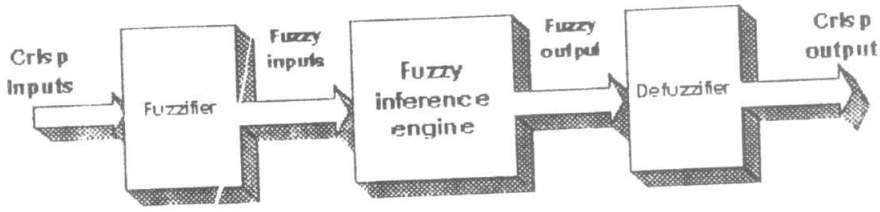

Fig. (1) Structure of a Fuzzy Logic Controller

The first stage of an FLC (the fuzzifier) converts crisp input data into fuzzy data represented by a value of a linguistic variable and a grade of membership in a fuzzy set. In this paper, an analog membership function circuit and its VLSI implementation are presented.

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FUZZIFICATION

The fuzzification block in an FLC involves a domain transformation where crisp inputs are transformed into fuzzy inputs . To do this, membership functions must be first determined for each input . Once membership functions are assigned , fuzzification takes a real-time input value such as temperature, pressure,...,etc.. and compares it with the predefined membership function information to produce fuzzy input values [5],[7].

The shape of a membership function affects the fuzzy process in subtle ways. For example , a function's shape directly affects the time and space requirements for fuzzification. Membership functions can take several different shapes; trapezoidal and triangular are most frequently used. Although other shapes (e.g. bell-shaped functions) may be more representative of natural occurring phenomena , they are generally more difficult to implement [6] .

THE BASIC MEMBERSHIP FUNCTION CIRCUIT

Basically , a fuzzy term can be defined by a membership function of trapezoidal shape as shown in Fig. (2)]. The core of the function corresponds to the region which has a full membership (μ =1). The ascending and descending boundaries are the regions with partial matching or membership ($0 < \mu < 1$) . The support of the defined fuzzy term is then the sum of the core and boundaries in which $\mu > 0$; where $\mu(x)$ is the membership function grade of input x [5],[7].

Commonly, four types of membership function are adopted in hardware design of fuzzy systems ; namely , S-shaped , Z-shaped , Triangular-shaped and Trapezoidal-shaped functions .

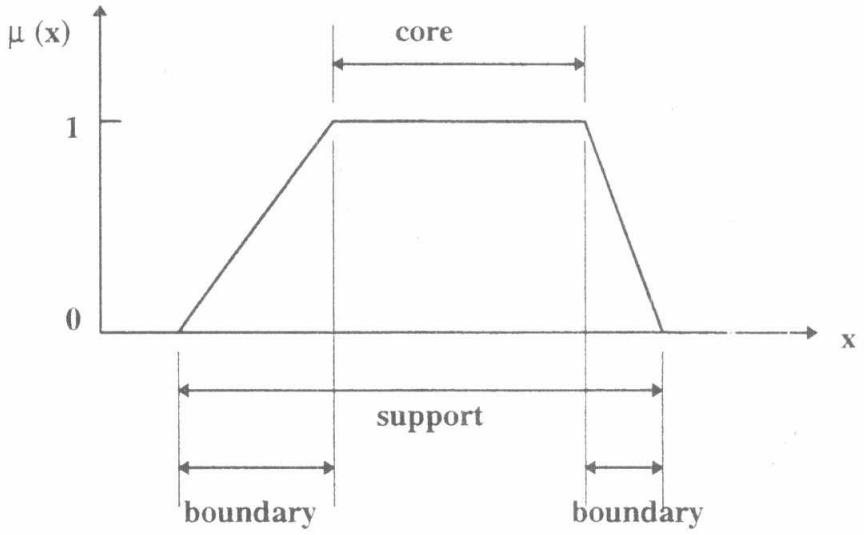

Fig. (2) Trapezoidal shape of a membership function

Various approaches have been proposed to generate analog nonlinear membership functions in either current or voltage mode [8],[9],[10] [11] . The base for our presented circuit is a membership function circuit (MFC) built of two differential pairs (DP1 and DP2) coupled with a common load as shown in Fig. (3) [8].

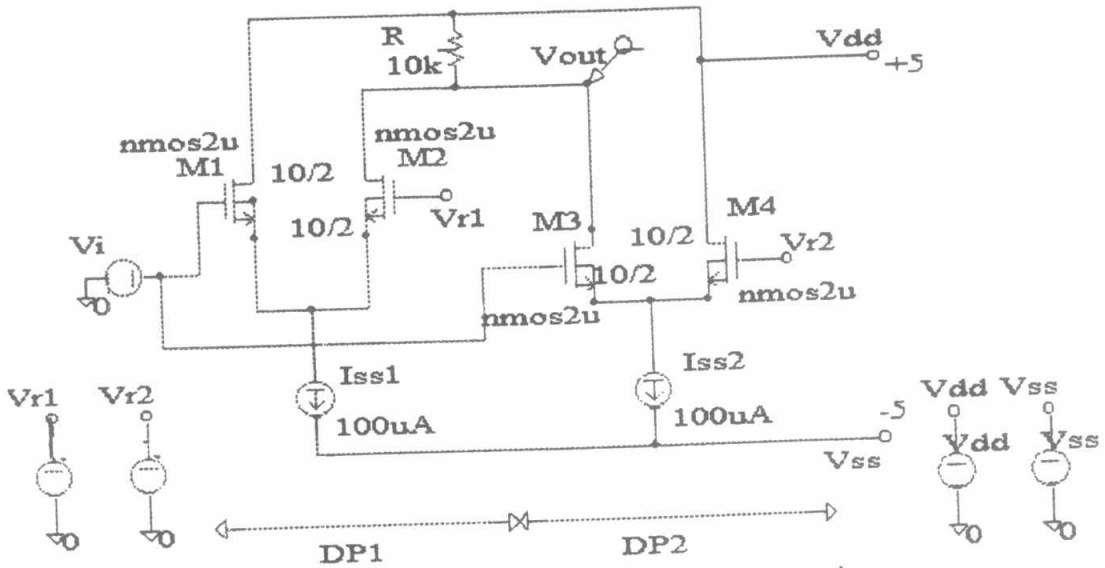

Fig. (3) Basic membership function circuit

CIRCUIT ANALYSIS

Depending on the relative values of the input voltage Vi and the reference voltages Vr1 and Vr2 , the circuit of Fig. (3) operates in one of the five regions (I to V) shown in Fig. (4).

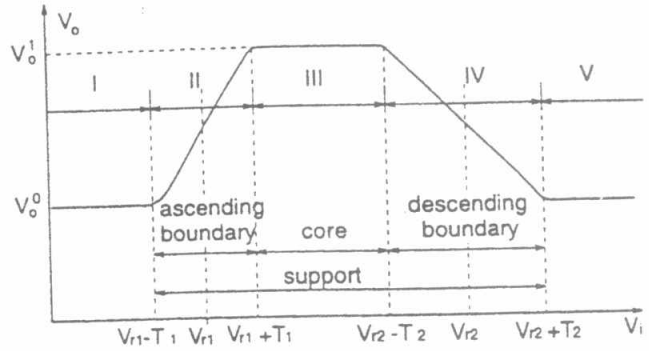

Fig. (4) The transfer characteristics of the membership function circuit

Assuming that the current sources Iss1 and Iss2 in DP1 and DP2 are ideal and identical (Iss1=Iss2=Iss), and the MOSFETs in each differential pair are matched, we can find the values of the input voltages of the ascending and descending boundaries related to Vr1 and Vr2 from the following equation:

$$T_j = \sqrt{\frac{2\mathbf{Iss}}{\beta_j}} \qquad j=1,2$$

where β_j is the transconductance parameter of the MOSFETs in DP1 and DP2 with j=1 and j=2 ; respectively [12].

The five operating regions of the MFC of Fig. (2) can be described as follows :

- *Region I :* $Vi < Vr1 - T1$,

Here M1 and M3 are in their cutoff regions while M2 and M4 are in saturation. The current through the load resistance R is equal to Iss . In this case, the output voltage is given by:

$$Vout = Vdd - Iss\ R = V_o^0$$

which corresponds to a membership function value 0.

- *Region II :* $Vr1 - T1 \leq Vi \leq Vr1+T1$, $Vr2-Vr1 \geq T1+T2$

Here, DP1 is in its transfer region while DP2 keeps the same state as in region I . As Vi increases in this region, the membership function circuit gives a linear ascending output which corresponds to a membership function value between 0 and 1.

- *Region III :* $Vr1+T1 < Vi < Vr2-T2$

Here both M1 and M4 are cutoff and the current flowing thro ugh the load R is zero. In this case, the output voltage is given by:

$$Vout = Vdd = V_o^1$$

which corresponds to a membership function value 1.

- *Region IV :* $Vr2 - T2 \leq Vi \leq Vr2+T2$

Here DP1 keeps the same state as in region III while DP2 operates in its transfer region ; antisymmetric to the case in region II. As Vi increases, the membership function circuit gives a linear descending output which corresponds to a membership function value between 1 and 0.

- *Region V :* $Vi > Vr2+T2$

Here the circuit operates as in region I but DP1 and DP2 have reverse roles . In this case the output voltage is V_o^0 which corresponds to a membership function value of 0 .

As shown above, the definition of the implemented MFC is dependent on the reference voltages Vr1,Vr2, transconductance parameters $\beta 1$ and $\beta 2$ of DP1 and DP2 and current Iss . By changing the values of these parameters in the circuit presented , the membership function can have different shapes , types , slopes and positions on the voltage axis (Universe of discourse) . For example, we can get a triangular shape when Vr1+T1 equals Vr2-T2 . The same function changes to an S- or Z-shape type if Vr1 is equal to the highest potential in the circuit (i.e.,Vdd) or Vr2 is equal to the lowest potential (i.e., Vss); respectively . The positive and negative slopes of the membership function are mainly determined by the transconductance parameter of the MOSFETs in DP1 and DP2 ; respectively.

THE MODIFIED CIRCUIT AND ITS VLSI IMPLEMENTATION

The use of resistors is usually avoided in the implementation of fully integrated analog MOS circuits. One of the main reasons is the unpredictability of the values. For polysilicon or diffused resistors, the fabrication process as well as temperature variations contribute to the uncertainty of resistor values which can be 20 % or more [13]. Also, for diffused and polysilicon resistors, the sheet resistance is low in value so that a high value resistor occupies a large area . In this paper we have modified the circuit of Fig. (3) so that the resistor R is replaced by a p-channel MOSFET with a constant voltage between gate and source ,Vgs, as shown in Fig (5) . This modification makes the circuit more suitable for VLSI implementation . Here, the output voltage of the circuit can be pulled up to Vdd thus :

$$V_{out}(max) \approx V_{dd}$$

Note that, an active load resistor (Diode connected transistor) is not suitable here as the maximum output voltage in this case would be :

$$V_{out}(max) = V_{dd} - V_t$$

where Vt is the threshold voltage of the load transistor.

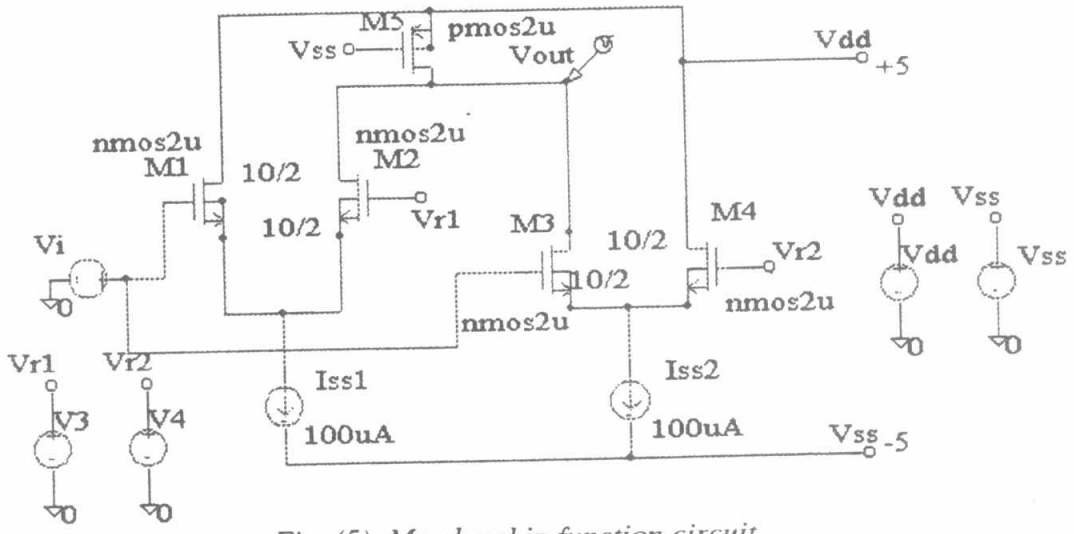

Fig. (5) Membership function circuit

Having concluded the description of the proposed membership function circuit, we'll present now an example showing how this circuit can be used to implement a practical three-term membership function .Figure (6) shows the 3-term membership function circuit and Fig.(7) shows its transfer characteristic obtained from PSpice simulation for the following voltage and current values:

Vdd=-Vss=5v	Vr1= -5v	Vr2=Vr3=1.5v
Vr4=Vr5=3.5v	Vr6=6v	Iss1 to Iss6 = 100 μA
(W/L)=10/2 for M1 to M12		(W/L)=6/5 for M13 to M15

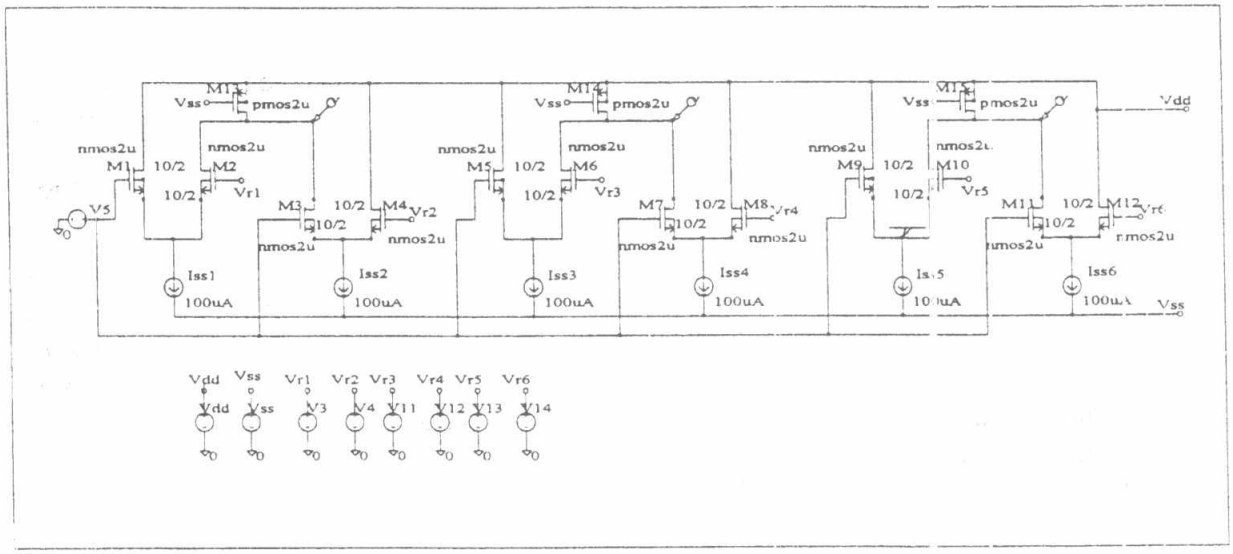

Fig. (6) The three term membership function circuit

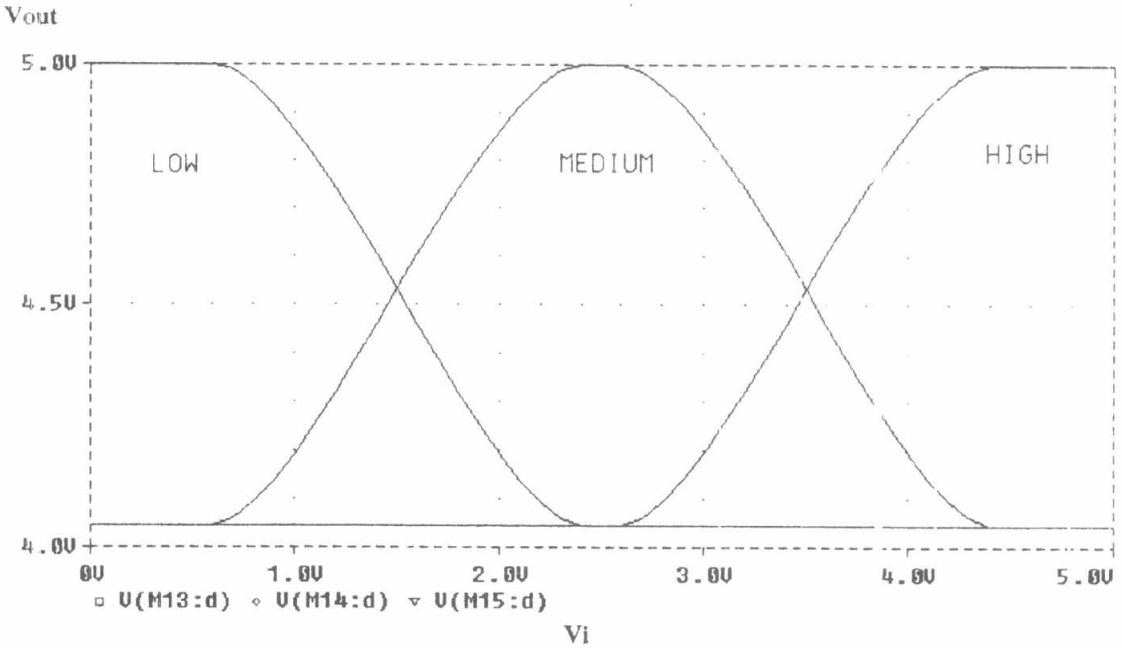

Fig. (7) The simulation results of the MFC of Fig.(6)

The VLSI layout design of the membership function circuit of Fig(5) was performed with the aid of the L-EDIT program Version 5.13. The design is based on the MOSIS's Orbit Semiconductor n-well 2.0 µm CMOS process with: technology = SCNA (Scalable CMOS N-well Analog) and Lambda =1.0 µm [14],[15]. The MOSIS service is a low-cost prototyping and small volume production service for custom and semi-custom VLSI circuit development. Figure (8) shows the resulting layout design which occupies a very small area of the silicon real estate (42 µm x 47 µm).

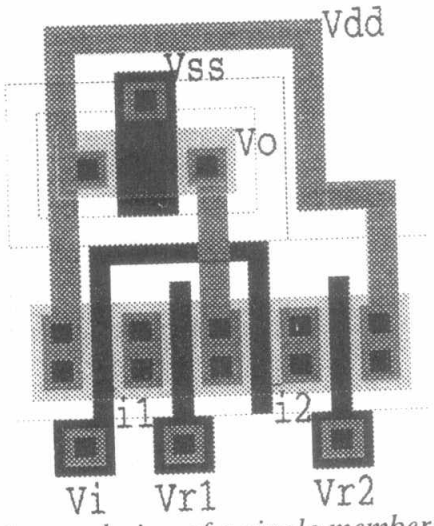

Fig. (8) VLSI layout design of a single membership function circuit

To test the layout design of Fig. (8) ,we have extracted a PSpice compatible circuit file which is produced by L-Edit V5.13/Extract V2.06 program. This file has then been simulated using PSpice , the simulation result is shown in Fig. (9). It is clear that the transfer function of Fig. (9) is the same shape of the membership function of Fig. (4) which proves the correctness of the design.

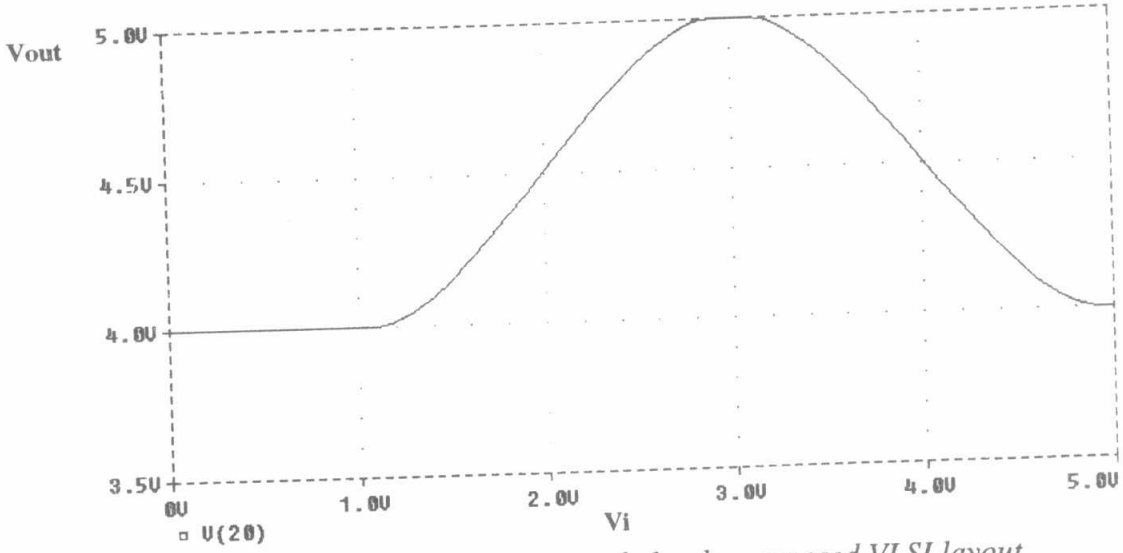

Fig. (9) Simulation result for the proposed VLSI layout

CONCLUSION

In this paper we have introduced a fully CMOS analog membership function circuit and its VLSI implementation. The implemented circuit consists of only five MOSFETs and occupies a very small silicon area. In addition, a practical three-term membership function circuit has also been introduced. The proposed design can be extended to provide any practical multi-term membership function. This analog circuit produce a Bell-shaped membership function which may be more representative of natural occurring phenomena .

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