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A NOVEL DESIGN OF AN FPGA-BASED REPROGRAMMABLE DIGITAL CLOCK GENERATOR

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ABSTRACT

This paper presents a novel design of an FPGA-based, reprogrammable digital clock generator that produces a group of clock signals with variable duty cycles. The realized chip provides up to fourty eight, independent, crystal-controlled, variable-duty-cycle clock outputs; each having a duty-cycle that can be varied from 0.4 % to 99.6 % in 250 steps. The proposed design can be used in a variety of applications. One of the main applications is the adjustment of the synaptic weights of an artificial neural network (ANN). The designed unit can also be used as the basis of a highly flexible pulse generator or a complex waveform generator.

INTRODUCTION

Recently, usage of Field-Programmable Gate Arrays (FPGAs) in realizing complex hardware systems has been accelerated [1]. Field-programmable gate arrays are high-density digital integrated circuits that can be configured by the user; they combine the flexibility of gate arrays with desktop programmability [2]. The relatively low-cost and easiness of implementation and programming of FPGAs in comparison with the custom VLSI technology offer attractive features to the designer. In this paper, we introduce a novel design of an FPGA-based, reprogrammable variable-duty-cycle clock generator. The available A1280A-PL84C FPGA chip, from Actel corporation, has been used in the implementation of our design [3]. This is an 84-pin, antifuse-based FPGA chip whose architecture depends on the PLICE (*Programmable Low-Impedance Circuit Element*) antifuse [4]. Eight-bit digital words, dynamically stored via an external computer into the FPGA chip, determine the values of the duty-cycles of the generated clocks.

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BASIC IDEA

The block diagram of the circuit implementing a single variable-duty-cycle output is shown in Fig. 1(a). The circuit operates as follows :
First, two 8-bit values M and N are stored in latch "1" and latch "2", respectively, by an external source. The values of M and N must satisfy the relation :

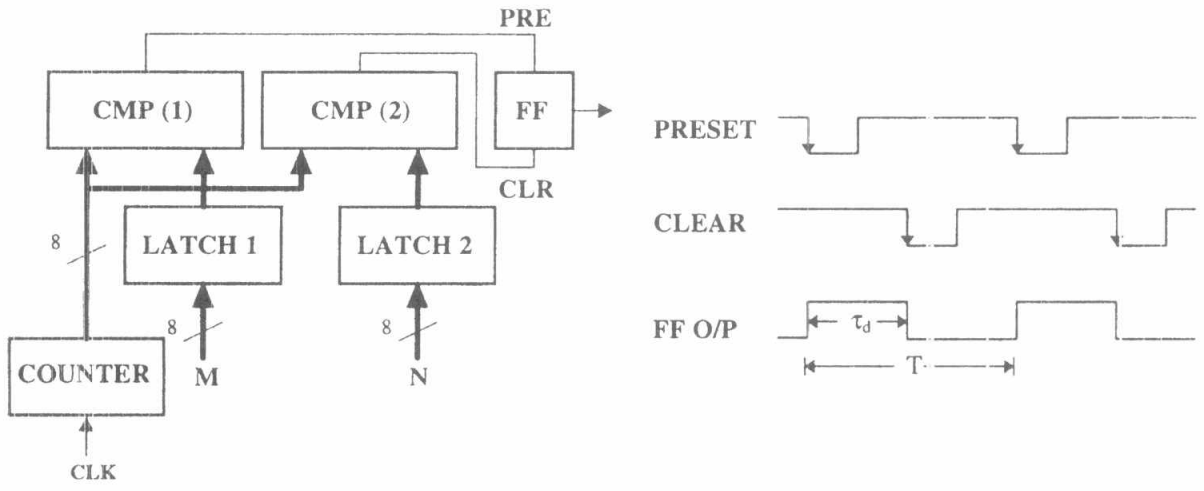
$$0 < N < M \tag{1}$$

An input clock is introduced to the 8-bit synchronous counter and the counter output is incremented until it reaches the value M, stored in latch "1"; in this case, the output of comparator "1" changes to logic "0" which presets the flip flop, and resets the counter. The counter, now, begins to count at the positive edge of the next clock cycle. When the counter output equals the value N, stored in latch "2, the output of comparator "2" goes LOW, which clears the flip flop. The flip flop is preset again by the output of comparator "1" as the counter output reaches the value M. In this way, the pulse duration τ_d, and the period T of the generated clock signal are given by :

$$\tau_d = N \times T_c , \tag{2}$$

$$T = M \times T_c \tag{3}$$

where, T_c is the period of the external clock (see Fig. 1(b)).



(a) Block diagram **(b) Timing diagram**

Fig. 1 Basic idea for generation of a single variable-duty-cycle clock signal

The actual design implementing a single variable-duty-cycle output is shown in Fig. 2. Eight-bit words are used to represent the values of M and N. The value of M can be chosen in the range from 2 to 255. In this case, the value of N can range from 1 to 254, thus enabling generation of clock signals with a very wide range of duty cycles. Note that in all cases, inequality (1) must be satisfied. If a high accuracy crystal-controlled clock is used, the

generated signals will be highly accurate. With 8-bit values for M and N, the duty cycles of the produced signals can have a resolution of better than 0.4 %. If the word length is increased, to 10 bits say, the resolution can be better than 0.1 %.

To verify the design, the circuit of Fig. 2 has been simulated on PSpice and the simulation results are shown in Fig. 3. In addition, the circuit of Fig. 2 has also been realized practically and the practical results coincide with the simulation results. The circuit of Fig. 2 is the basis for implementing the FPGA-based digital clock generator.

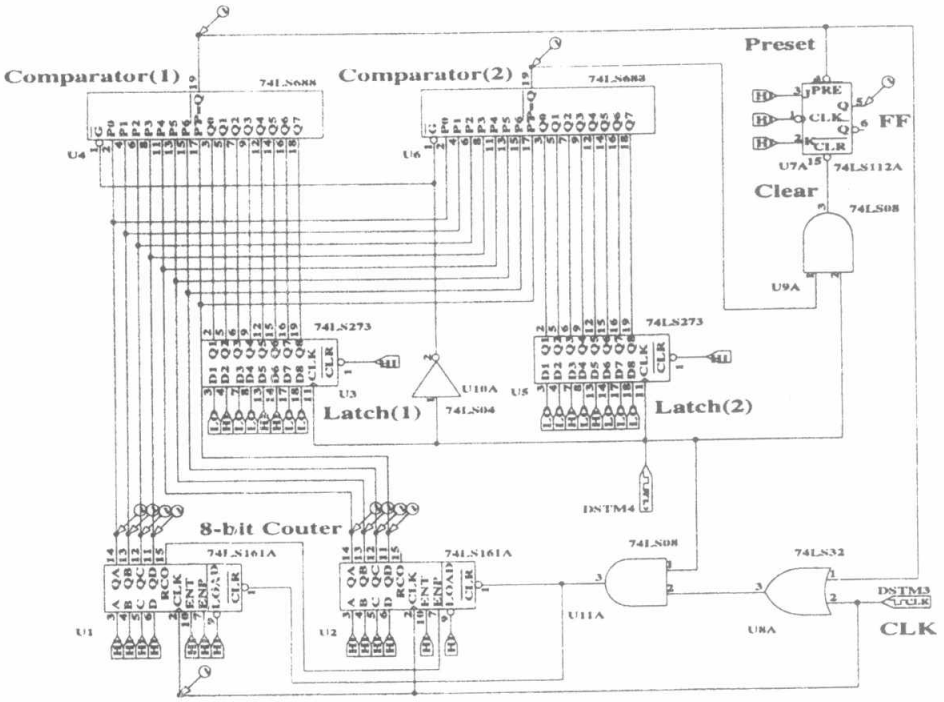


Fig. 2 Basic circuit for generation of a single variable-duty-cycle clock signal

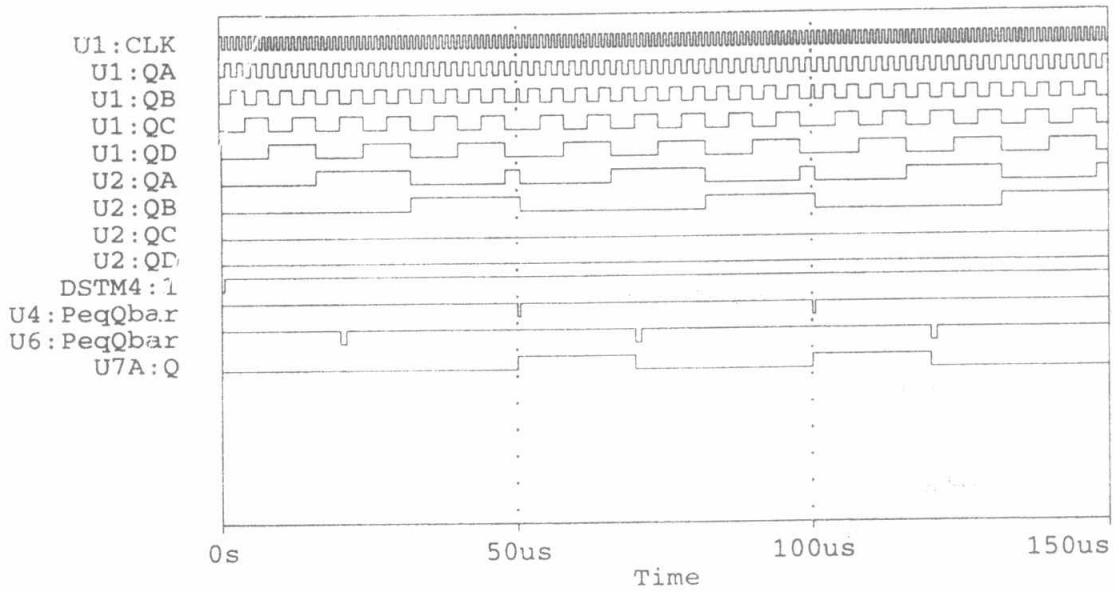


Fig. 3 PSpice simulation results for the circuit of Fig. 2

FPGA-IMPLEMENTATION

Here, we'll describe in detail the complete design of the presented 48-outputs digital clock generator.

(a) Block Diagram

The proposed design has the following inputs and outputs :

EIN1-EIN8 : 8 input lines carrying the 8-bit words that specify the period, and the duration values for each of the 48 variable-duty-cycle outputs. Fourty-nine bytes of data must be transferred through these lines to program the unit. These 49 bytes are stored in 49 latches; the first 48 latches contain the values representing the durations of the 48 output signals, and the remaining latch contains the value representing the period T.

EILS0-EILS6 : 7 input lines carrying latch select signals. Data presented on lines EIN1-EIN8, are stored in the selected latch.

The above mentioned 15 interface lines are all what is needed to program the digital clock generator by the external programming source.

CLK : an external clock signal, with a period T_c, that determines the timing of the whole unit.

MASTERCLR : an external input that can be used to reset all the outputs of the unit to a predefined state.

All the above inputs are buffered prior to being introduced to the internal circuitry of the unit.

OUT0-OUT47 : 48 independent, reprogrammable, variable-duty-cycle buffered outputs.

(b) Circuit Description

Since our design has been first realized using conventional SSI/MSI logic components, we had first to convert these components to corresponding FPGA macros obtained from the Actel Macro Library Guide [5]. Fig. 4 shows the circuit diagram of the FPGA chip drawn using the "*Viewlogic*" schematic capture (PROcapture) software. The circuit consists of :

(1) An eight-bit synchronous binary counter with an external clock.

(2) An octal positive-edge triggered latch.

(3) An 8-bit magnitude comparator.

(4) An inverter and a group of buffers.

(5) Six identical macros, each comprising the following (see Fig. 5) :

(i) Eight octal positive-edge triggered latches.

(ii) Eight 8-bit magnitude comparators.

(iii) Eight D-type flip flops with active high preset and active low clear.

(iv) Eight AND gates.

(6) A 1 of 64 decoder enclosed in a macro consisting of nine 3×8 Actel decoders with enable.

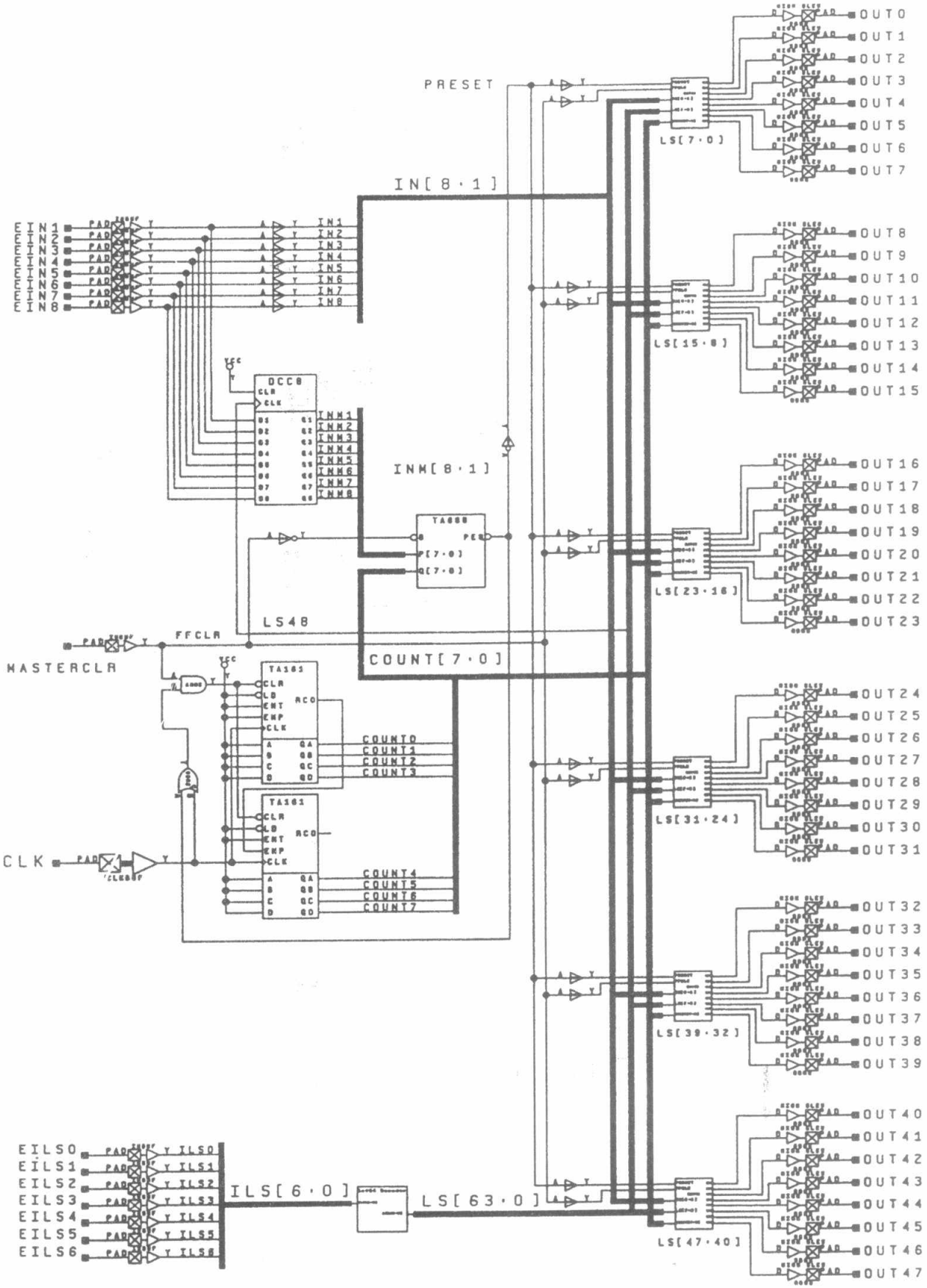


Fig. 4 The FPGA chip circuit diagram

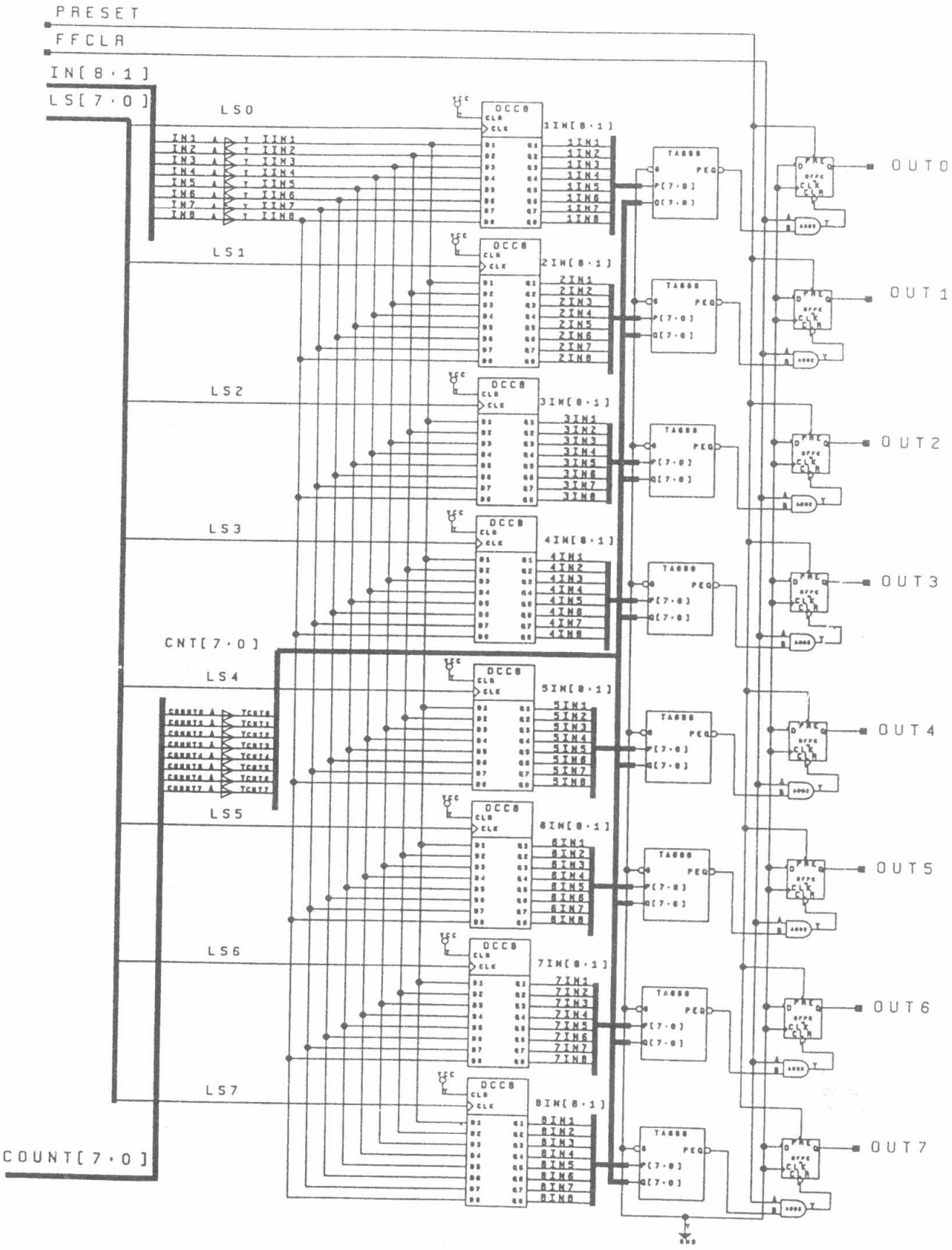


Fig. 5 The FPGA macro circuit diagram

(c) Simulation Results

The FPGA design has been simulated using the *"Viewlogic"* simulation program (PROsim). To achieve this, a simulation file has been written to tell the program such information as the value of the clock frequency, the initial states of the flip flops, the values to be stored in the latches, and the waveforms to be displayed. Fig. 6 shows the waveforms resulting from the simulation for the first 8 output pins of the chip for duty cycles of 1/36, 2/36, 5/36, 7/36 8/36, 22/36, 32/36, 35/36, respectively.

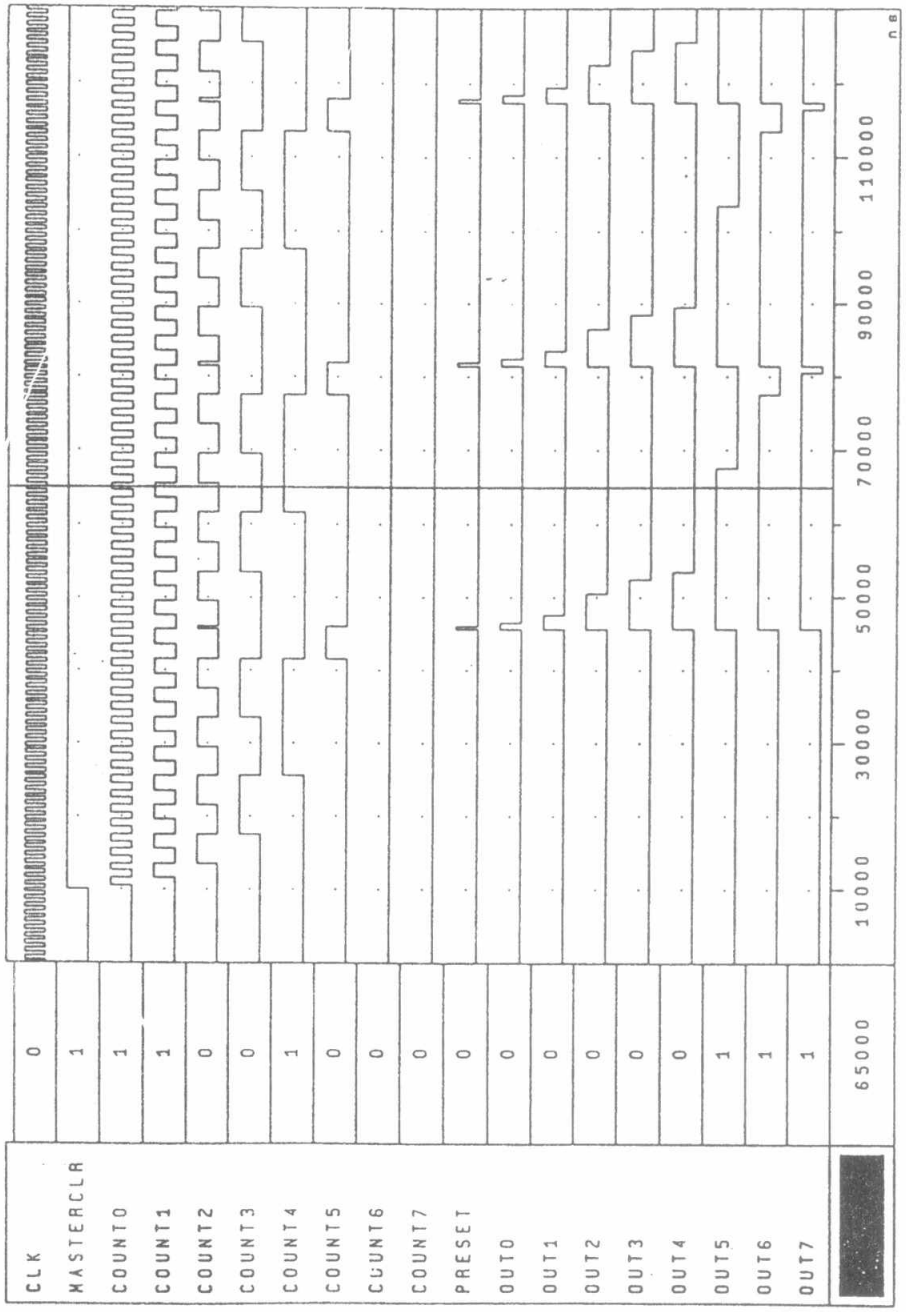


Fig. 6 Simulation results of the FPGA chip

A PRACTICAL APPLICATION

The above designed digital clock generator has been actually applied as a digital control unit for adjusting the synaptic weights of a hybrid ANN as presented in [6]. The synaptic weights are represented by switched CMOS transistors whose "on" resistances are proportional to the duty cycles of the switching clocks. A single synaptic weight circuit is shown in Fig. 7. The high resolution of the generated clock signals increases the accuracy of the realized weights.

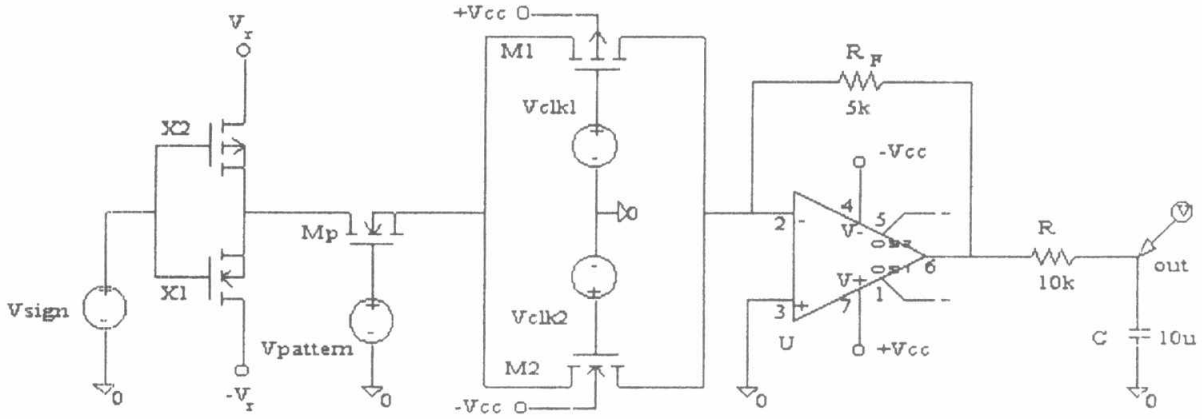
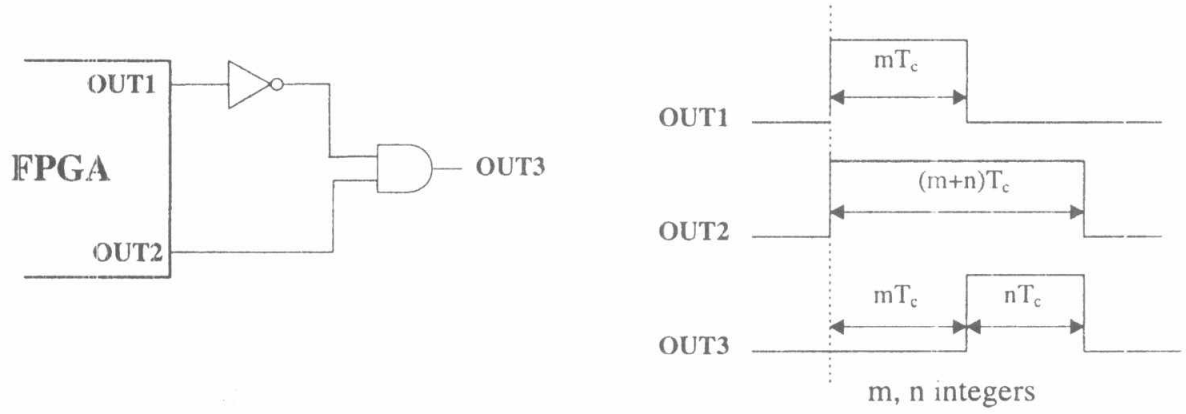


Fig. 7 A synaptic weight circuit

OTHER APPLICATIONS

Due to the high flexibility and versatility of the design, its use can be extended to several applications. For example, combining two outputs of the clock generator, as shown in Fig. 8(a), produces a periodic pulse with arbitrary width and arbitrary position, as shown in Fig. 8(b), which may find application in digital communications. Combining more than two outputs with the help of a few combinational logic circuits, much more complex pulse signals and waveforms may be obtained.



(a) Circuit diagram **(b) Timing diagram**

Fig. 8 A pulse with programmable width and position

CONCLUSION

A highly flexible and versatile, FPGA-based, reprogrammable digital clock generator that produces 48 independent clock signals with variable duty cycles has been presented. It makes use of 8-bit digital words to produce clock signals with duty cycles adjustable in 256 steps (2^8), thus achieving a resolution of better than 0.4 %. It may be used in a variety of applications. A typical application of the designed FPGA chip, in controlling the values of the synaptic weights of an ANN, has been introduced. The designed chip can also be the basis of highly flexible pulse generators or complex waveform generators.

REFERENCES

[1] Nazeih M. Botros, and M. Abdul-Aziz, "Hardware Implementation of an Artificial Neural Network Using Field Programmable Gate Arrays (FPGA's)," *IEEE Transactions on Industrial Electronics*, vol. 41, no. 6, pp. 665-667, December 1994.

[2] Stephen M. Trimberger, '*Field-Programmable Gate Array Technology*,' Kluwer Academic Publishers, Massachusetts, USA, 1994.

[3] Actel, '*FPGA Data Book and Design Guide*,' Actel, 1994.

[4] J. Greene, E. Hamdy, S. Beal, "Antifuse Field Programmable Gate Arrays," *Proceedings of the IEEE*, vol. 81, no. 7, pp. 1042-1056, July 1993.

[5] Actel, '*Macro Library Guide*,' Actel, 1995.

[6] Hesham N. Mohamed, '*Circuit Implementation of Neural Networks*,' M. Sc. Thesis, Military Technical College, Egypt, 1997.