Military Technical College
Kobry Elkobbah,
Cairo, Egypt

ICEENG 99

2nd International Conference
on Electrical Engineering
ICEENG 99

Standard VLSI Cells For Fuzzy Logic Controller Implementation

A. K. Taha* A. S. Badawi** M. M. El-Khatib***

ABSTRACT

The VLSI CAD technology has been used for development of fuzzy logic based electronic hardware. Most of the existing standard cell liberties commercially available from various VLSI CAD vendors do not include any generic standard cells library to support fuzzy logic hardware. In this paper VLSI standard cells for a membership function circuit , Max circuit, Min circuit and defuzzification circuit are introduced.

KEY WORDS

Fuzzy logic controller, Standard fuzzy cells, VLSI implementation.

INTRODUCTION

DURING the sixties, Professor Lotfi Zadeh, of the University of California at Berkeley, put forward the proposition that vagueness is an aspect of uncertainty that is different from randomness. He proposed a mathematical way of looking at the intrinsic vagueness of the natural human language; he called his approach "fuzzy logic". The objective of fuzzy logic has been to make computers "think" like humans and remove the barrier between us and the full utilization of computer capabilities.

Fuzzy control is based on fuzzy logic; a logical system that is much closer in spirit to human thinking and natural language than traditional logical systems. The fuzzy logic controller (FLC), based on fuzzy logic, provides a means of converting a linguistic control strategy based on expert knowledge into an automatic control strategy [1],[2]. The basic configuration of an FLC, shown in Fig. (1), consists of three main components that are used to reach a crisp solution to a specific problem [3],[4].

---

* Ph.D., Dpt. of Elect. Eng., M.T.C.
** Asst. Prof., Faculty of Eng., Cairo University
*** Teach. Asst., Dpt. of Elect. Eng., M.T.C.

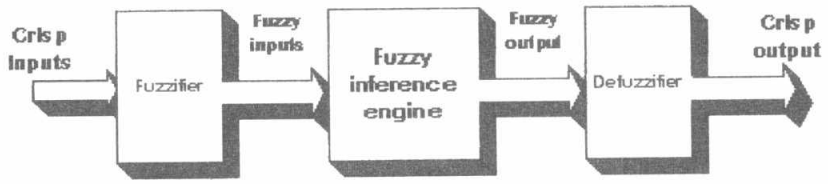


Fig. (1) Structure of a Fuzzy Logic Controller

Various approaches have been proposed to implement fuzzy controllers in either software or hardware. Hardware implementation of fuzzy logic is the solution to applying fuzzy logic techniques in real time complex applications. In this paper standard VLSI cells that can be used in hardware implementation of fuzzy controllers are introduced.

THE NEED FOR STANDARD CELLS IN FUZZY LOGIC HARDWARE

The VLSI CAD technology has been used for the development of fuzzy logic electronic hardware. Most of the existing standard cell liberties commercially available from various VLSI CAD vendors (Compass VTI, Mentor Graphics, Synopsys, ViewLogic, etc.) do not include any generic standard cells library to support fuzzy logic devices to give boost to VLSI designers engaged in fuzzy logic hardware development. The standard cells may be designed such that minimum silicon area achieved as possible without affecting the precision requirement. The standard cell library may include : min. and max. circuits, membership function circuit, defuzzification circuit (weightage block), etc [5]. In the next section, a small effort towards fuzzy logic cell standards is introduced.

MEMBERSHIP FUNCTION CELL

The fuzzification block in an FLC involves a domain transformation where crisp inputs are transformed into fuzzy inputs . To do this, membership functions must be first determined for each input . Once membership functions are assigned , fuzzification takes a real-time input value such as temperature, pressure,...,etc., and compares it with the predefined membership function information to produce fuzzy input values [6],[7].

The shape of a membership function affects the fuzzy process in subtle ways. For example , a function's shape directly affects the time and space requirements for fuzzification. Membership functions can take several different shapes; trapezoidal and triangular are most frequently used. Although other shapes (e.g. bell-shaped functions) may be more representative of natural occurring phenomena , they are generally more difficult to implement [8] .

Figure (2) shows a proposed membership function circuit which based on two differential pairs (DP1 and DP2) coupled with a common active load [9]. The definition of the implemented MFC is dependent on the reference voltages Vr1,Vr2, ransconductance parameters $\beta 1$ and $\beta 2$ of DP1 and DP2 and current Iss. By changing the values of these parameters in the circuit presented , the membership function can have different shapes, slopes and positions on the voltage axis (Universe of discourse).

For example, we can get a triangular shape when Vr1+T1 equals Vr2-T2 where T_j is the value of the input voltage of the ascending and descending boundary related to Vr1 and Vr2 from the following equation:

$$Tj = \sqrt{\frac{2Iss}{\beta_j}} \qquad j=1,2 \qquad (1)$$

where β_j is the transconductance parameter of the MOSFETs in DP1 and DP2 with j=1 and j=2 ; respectively [12] and the current sources Iss1 and Iss2 in DP1 and DP2 are ideal and identical (Iss1=Iss2=Iss).

MEMBERSHIP FUNCTION CIRCUIT

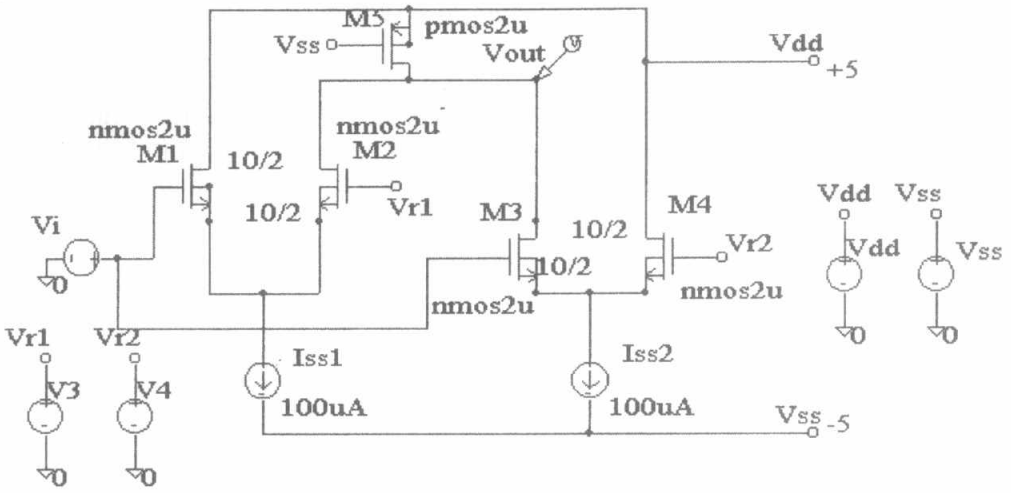


Fig (2) The membership function circuit

The same function changes to an S- or Z-shape type if Vr1 is equal to the highest potential in the circuit (i.e.,Vdd) or Vr2 is equal to the lowest potential (i.e., Vss); respectively . The positive and negative slopes of the membership function are mainly determined by the transconductance parameter of the MOSFETs in DP1 and DP2 ; respectively as shown in Fig (3).

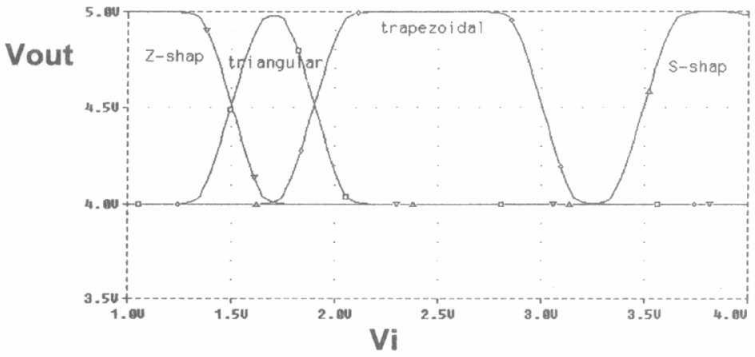


Fig. (3) Four types of membership functions

The VLSI layout design of the membership function circuit of Fig(3) was performed with the aid of the L-EDIT program Version 5.13. The design is based on the MOSIS's Orbit Semiconductor n-well 2.0 μm CMOS process with: technology

= SCNA (Scalable CMOS N-well Analog) and Lambda =1.0 μm [10],[11]. The layout design is optimized manually to have min silicon area (42 μm x 47 μm).

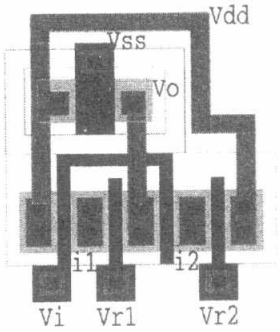


Fig. (4) VLSI layout design of a single membership function circuit

To test the layout design of Fig. (4) ,we have extracted a PSpice compatible circuit file which is produced by L-Edit V5.13/Extract V2.06 program. This file has then been simulated using PSpice , the simulation result is shown in Fig. (5). It is clear that the transfer function of Fig. (5) implement a membership function with trapezoidal shape.

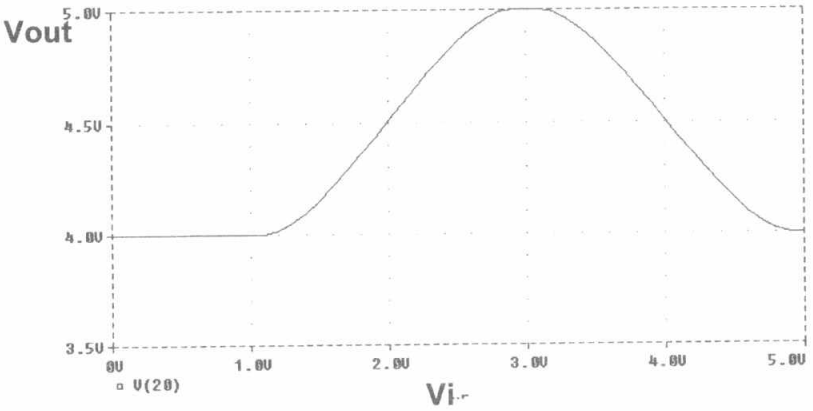


Fig. (5) Simulation result for the proposed VLSI layout

MIN AND MAX CELLS

The fuzzy inference engine is the heart of the fuzzy logic controller. Using Mamdani's inference technique, the inference is completed by a set of intersection and union operations which are realized by minimum (min) and maximum (max) circuits. These circuits are implemented using CMOS analog technology in voltage mode as shown in Fig. (6). The two-input max circuit consists of two NMOS devices M_1 , M_2 and a current source I_{ss} realized by a single MOSFET M_3. Two inputs are connected to the gates of M_1 and M_2 separately, the output V_{max} which is connected to the common source of the input devices, has always the bigger value of the two inputs V_1 and V_2 with an offset voltage V_{off}

$$V_{max} = \max (V_1 , V_2) \pm V_{off} \qquad (2)$$

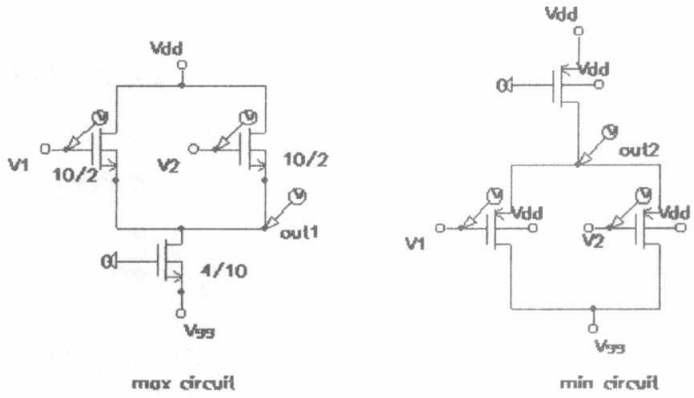


Fig. (6) The Basic Structure of the Two-input max and min Circuits

Figure (7) shows the simulation results of the circuits on Pspice

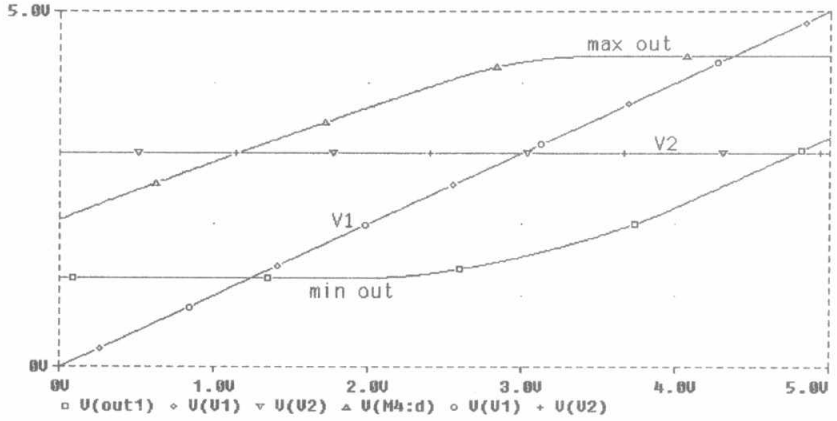
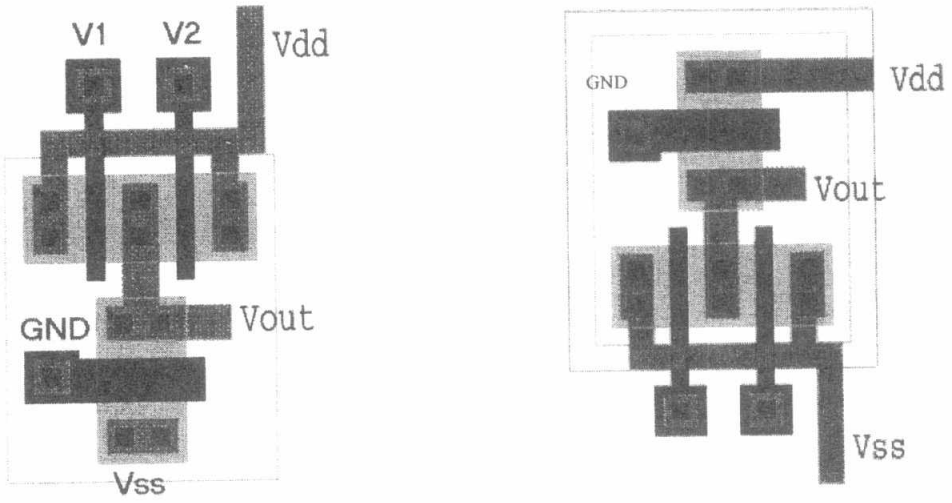


Fig. (7) The simulation results of the max and min circuits

Symmetrically, a min operator can be easily implemented by using PMOS devices. As indicated in Fig. (8). The output voltage of this circuit is

$$V_{min} = \min (V_1 , V_2) \pm V_{off} \qquad (3)$$

The VLSI Layout of the max and min cells are designed to achieve minimum area and similarity as shown in Fig.(8)



(a) Max cell *(b) Min cell*

Fig.(8) The VLSI layout of the max and in cells

DEFUZZIFICATION CELL (WEIGHTAGE BLOCK)

The output of a fuzzy inference engine is a fuzzy set which represents the possible distribution of the control action. For practical use, crisp control output is usually required. Thus a defuzzification inference is necessary to convert the inferred fuzzy control action into a non-fuzzy (crisp) value.

Among the suggested defuzzification strategies, the center of gravity (COG) method is the most commonly used. In the case of a discrete universe, the crisp output variable (Z) can be calculated as :

$$Z = \frac{\sum_{i=1}^{K} \mu_C(z_i) * z_i}{\sum_{i=1}^{K} \mu_C(z_i)} \qquad (4)$$

Where : K is the number of discrete fuzzy elements; $\mu_C(z_i)$ is the inferred (or final)membership function related to the i^{th} singleton z_i in the consequent z. i.e. the weight of z_i for the final output computation.

The theoretical analysis and experimental results have proved that the COG strategy has good steady state performance. An FLC based on the COG method generally yields lower mean square error than that based on other methods [12].

Several solutions have been proposed to build defuzzification circuits with COG method [13]. In most cases, a division circuit is used. However, this needs a relatively large design area. To avoid this, a defuzzification circuit which calculates the center of gravity without employing a division circuit is shown in Fig (10)[14]

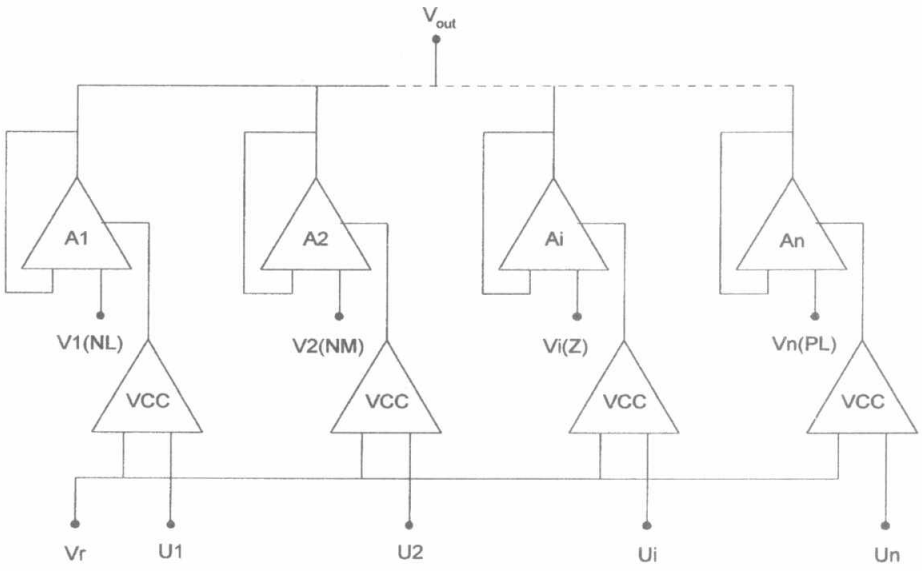


Fig.(10) The defuzzification circuit

As shown in the above figure the implementation is based on the a voltage follower-aggregation circuit. For a K-term defuzzification, K transconductance amplifiers (A_1 to A_K) are used to aggregate the input V_1 to V_K. They represent the values of K singleton terms in the consequence part of the fuzzy inference system. Assume that the transconductance of an amplifier A_i is G_i , i.e. G_1 for A_1 , G_2 for A_2 ....., G_K for A_K , then the current from the i^{th} amplifier A_i to the common point V_{out} is :

$$I_i = G_i (V_i - V_{out}) \qquad (5)$$

Based on Kirchhoff's current law, the sum of the current I_i coming from the K-amplifiers is zero. Thus we have :

$$V_{out} = \frac{\sum_{i=1}^{K} G_i * V_i}{\sum_{i=1}^{K} G_i} \qquad (6)$$

This means that the output voltage of the circuit V_{out} is the average of the inputs V_i. The contribution of each input to the output is weighted by the transconductance of the corresponding amplifier G_i ,where :

$$G_i = \left.\frac{\partial I_{oit}}{\partial V_{id}}\right|_{V_{id}=0} = \left(\frac{k' I_{ss} W}{L}\right)^{1/2} \qquad (7)$$

as $I_{ss} \equiv I_i$ input current to the transconductance amplifier
K' transconductance parameter
W width of the input device
L length of the input device

This means, the tranconductance G_i of an amplifier operates in its linear region, and that a voltage-current converter (VCC) circuit converts an input voltage U_i into a current I_i with a square law, as shown in Fig. (11) which shows the complete circuit of defuzzification cell

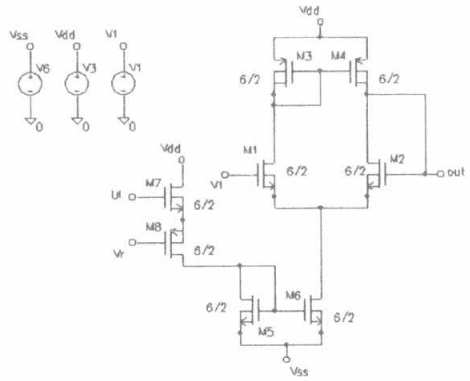


Fig (11) The defuzzification cell

Thus, it can be written as follow :

$$I = \frac{\beta_{eq}}{2}\left(V_{GSeq} - V_{theq}\right) \qquad (8)$$

Where : $V_{GSeq} = V_{GSn} + V_{GSp}$

$$V_{theq} = V_{thn} + V_{thp}$$

$$\beta_{eq} = \frac{\beta_n \beta_p}{\left(\sqrt{\beta_n} + \sqrt{\beta_p}\right)^2}$$

So, by substituting V_{GSeq} in Eq.(8) by $(U_i - V_r)$ and choose the reference voltage Vr to be equal Vtheq , it can be rewritten as :

$$I = \frac{\beta_{eq}}{2} U_i^2 \qquad (9)$$

Then the output of the defuzzification circuit will be :

$$V_{out} = \frac{\sum_{i=1}^{n} U_i * V_i}{\sum_{i=1}^{n} U_i} \qquad (10)$$

The layout of the defuzzification cell under consideration of minimum area is shown in Fig.(12)

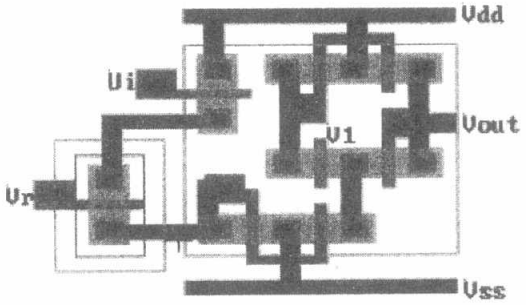


Fig (12) VLSI layout of the defuzzification cell

CONCLUSION

A step towards VLSI standard cells for fuzzy logic based systems has been achieved here. Although the VLSI CAD technology has been used for development of fuzzy logic based electronic hardware, until now, most of the existing standard cell liberties commercially available from various VLSI CAD vendors do not include any generic standard cells library to support fuzzy logic hardware So we introduce a suggestion for standard cells for Membership function circuit, Min circuit, Max circuit (which used in inference engine design) , and Defuzzification circuit.
The introduced cells have the following features :

- Small silicon area.
- Modularity.
- Versatility.
- Full CMOS implementation.

REFERENCES

[1] C. C. Lee,'*Fuzzy Logic in Control Systems: Fuzzy Logic Controller ,Part* I' IEEE Trans. Syst. Man Cybern. Vol. 20 No. 2,1990.

[2] C. C. Lee,'*Fuzzy Logic in Control Systems: Fuzzy Logic Controller ,Part II*' IEEE Trans. Syst. Man Cybern. Vol. 20 No. 2,1990.

[3] A. M. Ibrahim ,' *Introduction to Applied Fuzzy Electronics* ' ,Prentice Hall Inc. ,1997

[4] M. J. Patyra and D. M. Mlynek ,' *Fuzzy Logic Implementation and Applications* ' , John Wiley & Sons Ltd.and B.G. Teubner ,1996

[5] A. B. Patki *"Fuzzy Logic Based Hardware : Some Experiences"*Electronics Information & Planning Journal , vol. 21, No 4, January, 1997.

[6] Center Of Engineering Computer Technologies, MOTROLA Inc. ,' *Fuzzy Logic Education Program* ' , Software By Cortex Communications Inc.,Austin,Texas, 1992.

[7] M. Jamshidi ,N. Vadiee and R. Timothy ' *Fuzzy Logic and Control* ' Prentice-Hall Inc.,1993 .

[8] H. T. Nguyen and E. A. Walker ,' *A First Course in Fuzzy Logic* ' , CRC Press Inc. ,1997

[9] Abdalla Khodair, Amr Badawy and Mohamed El-khatib "*VLSI Implementation of Fuzzy Logic Membership Function Circuit*", Proceeding of the 1st ICEENG Conference, March 1998.

[10] M. R. Haskard and I. C. May '*Analog VLSI Design; nMOS and CMOS*' Prentice Hall Inc. ,1988 .

[11] J. P. Uyemura '*Physical Design of CMOS Integrated Circuits Using L-EDIT™*, PWS Publishing Company ,1995 .

[12] Clarence W. de Silva '*Intelligent Control Fuzzy Logic Applications*', CRC Press, 1995.

[13] C. Y. Chen, C. Y. Huang, and B. D. Liu, "*Current-Mode Defuzzification Circuit To Realize The Centroid Strategy*" IEE Proc.- circuits devices syst., vol. 144, No.5, OCTOBER, 1997.

[14] Sh. Guo, L. Peters, "A New Hardware Implementation of the Center of Gravity Defuzzification Method" Vorträge der 3. GI/ITG/GME-Fachtagung : Rechner-gestützter Entwurf und Architektur mikroelektronischer Systeme, pp 145-150, Oberwiesenthal, Mai 1994.