A DUAL MODULATION PULSE POSITION MODULATION APPROACH IN 130NM CMOS TECHNOLOGY FOR TIME BASED SERIAL COMMUNICATION LINKS

Mostafa SalahRashdan[a] ,Nesma M. Sobhy[b] ,Ahmed El-Sawy[c]
[a]Electrical Engineering Dept, Faculty of Engineering, Aswan University,mabdelha@aswu.edu.eg
[b] Electrical Engineering Dept., Faculty of Engineering, Minia University,
nesma_20108784@yahoo.com
[c]Electrical Engineering Dept., Faculty of Engineering, Minia University

Abstract—A time-based serial data link architecture that involves dual modulation Pulse Position Modulation approach (DMPPM) is presented in this paper. In the proposed approach, both the rising and falling edges of the input clock signal are modulated independently. Using the proposed approach allows increasing the total number of transmitted bits without significantly affecting the modulated signal bandwidth. A 6-bit 4.8 Gb/s DMPPM link design example has been designed and simulated based on the proposed approach in 130nm CMOS technology. An 800MHz has been used as an input clock signal. The simulation results and a comparison between the proposed link and other serial links are presented. The power consumption of the transmitter and the receiver circuits are less than 100mW.

Keywords— *PPM, TDC, dual modulation, time resolution.*

I. INTRODUCTION

The requirements for designing serial links have increased as the demand for multi Gb/s data communication has continually increased tremendously. There are more limitations on such links due to CMOS technology scaling that have been inflexible with the increasing in the data rate. The loss channel one of these limitations, which cause an inter-symbol interference (ISI) and severely attenuate the transmitted signal. An increasingly complex equalization techniques need to be implemented in the transmitter and receiver to offset the losses of this frequency-dependent channel as presented in[1-3]. Furthermore, as the frequency increase, the constituent circuits of both transmitter and receiver in the serial link are increasingly complicated due to the appearance of a crosstalk, jitter, data skew and ISI.

The transceiver circuit of a serial link consists of a transmitter side, a transmission channel, and a receiver sideFig.1 illustrates a prevalent block diagram of a generic serial link. The input bits are serialized into a stream of data which is pre-emphasized at the end of the transmitter circuit and transmitted through a bandwidth-limited transmission channel. At the receiver side, the received data is equalized to offset the weakness caused by the channel to the transmitted signal. Then, a clock and data recovery (CDR) circuit is used to extract the clock and data. Finally, the extracted data is sampled by the recovered clock and de-serialized back into a set of parallel signals.

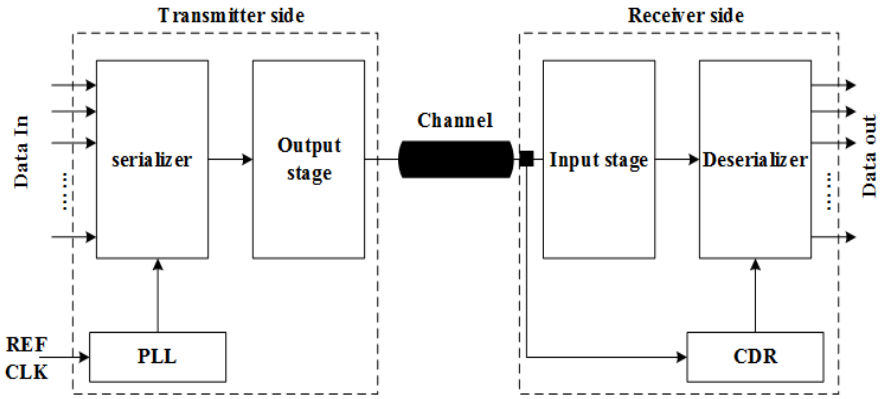

Fig.1. The generic block diagram of a serial link.

At high data rate, these architectures consume much power and area on the chip due to using more complicated circuits such as phase-locked loop (PLL) circuit and the clock and data recovery circuit (CDR). Furthermore, an inter-symbol interference (ISI) effects[4]caused by transmission line reflections in transmission media (channel) are increased, these increases the difficulty of links and the challenges on designers.

Different types of modulation techniques have been used to implement various serial links to face the challenges which appeared from the increase of the data rate. A pulse amplitude modulation is one of the modulation techniques, where the data rate of the transmitters amount to several gigabits per second [5]. Because the scaling of CMOS technology has been increased, the circuit's voltage headroom has been highly reduced. As a result, multi-level PAM techniques have a miserable voltage resolution and insufficient resilience for more bits are added to the link. Therefore, they are undesirable reduces the effect of clock jitter, relaxes the circuit design and uses much lower input clock frequency than the multiplexing serial links, such as embedded clock Serializes/Desterilized (SerDes) links, which is utilized to relieve the link design and less power consumption. As a consequence, a lower bandwidth is occupied by the transmitted signal which makes it distinct from all types of the SerDes links. There are two basic time-based modulation techniques: the pulse width modulation (PWM) technique is one of them and the other is the pulse position modulation PPM technique.

In [6], a CMOS 400-Mb/s interface circuit with PWM scheme was presented. To reduce the pin count, the data and clock channels were joined in a single channel. The binary data is encoded into pulses with different widths where as guaranteeing a periodic rising edge during each period. For recovering the clock signal easily in the receiver, a phase-locked loop(PLL) is used. At high frequencies, the period of the clock is decreased. Subsequently, the pulse width now has a very limited range. Using a PLL for generating time-shifted sampling clocks complicates the design especially at high frequencies. In[7],the PWM technique has been combined with the PAM technique in order to increase the number of the data bits and as a result increasing the data rate of the transmitted data signal. So that the authors achieved high data rate transfer using both PWM and PAM (PWAM) schemes.

Given the obliged limitations of CMOS technology scaling on the PAM and PWM, a time-based PPM-TDC architecture was presented in [8-12] and is shown in Fig.2. The authors displayed a low power time-based serial link employing a PPM modulation technique. The presented architecture utilizes only one modulation approach and separates the clock from the data then they are transmitted over two separate channels. The introduced architecture in [8, 9]overcomes the disadvantages of other serial links. The PPM technique has many benefits over the PWM such as power consumption, achievable data rate, transceiver circuit simplicity, and chip area. So that, our focus in the proposed link about using two PPM architectures at the transmitter and a two TDC at the receiver for designing a serial data link to increase the number of transmitted bits without complicating the link and to low power consumption.

This paper is organized as follows: Section II shows the design details of the Dual Pulse Position Modulation (DMPPM) architecture, Section III shows the simulation results for the proposed link. Finally, section IV concludes the presented work in this paper.

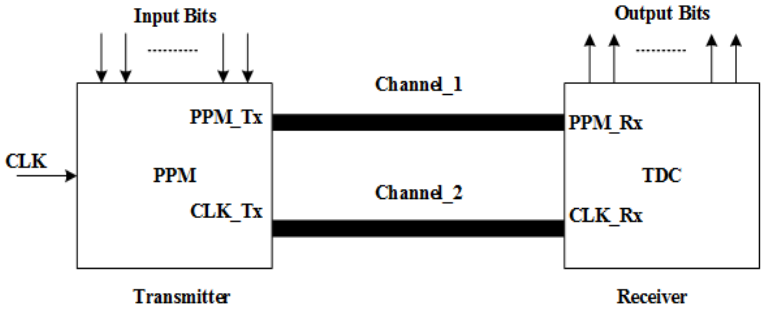

Fig.2.The block diagram of the PPM-TDC serial link [8,9].

II. DESIGN DETAILS

The proposed DMPPM approach is shown in Fig. 3 and Fig. 7. The approach of the proposed link is based on using a two-pulse position modulator (PPM) circuits as a transmitter and a two time-to-digital converter (TDC) as a receiver. In the proposed approach, both the rising and falling edges of the input clock signal are modulated independently. The proposed link allows increasing the total number of transmitted bits without significantly affecting the modulated signal bandwidth compared to other PPM approaches. the benefit of the proposed architecture is enhancing the time resolution in scaled CMOS, instead of a miserable voltage resolution. The proposed link utilizes uncomplicated circuitry which leads to less power consumption and increasing the number of transmitted bits.

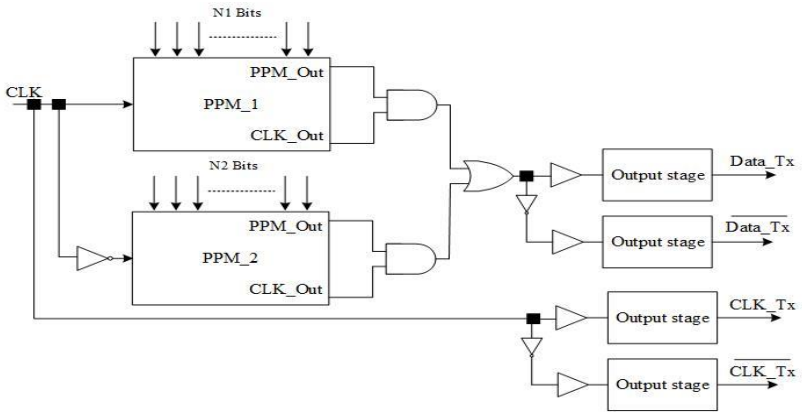

Fig.3.The block diagram of the transmitter side of the proposed architecture.

A. The Transmitter Circuit

As shown in Fig.3, the transmitter of the proposed approach utilizes the generation of one signal with both edges modulated. Two hierarchal PPM circuits are used in the transmitter circuit design which were presented in[13]due to its advantages related to power consumption, circuit simplicity, and single-cycle-latency.

Generally, in the PPM circuit, the input data is encoded into a time difference between the positive or negative edge of the clock pulse and the positive or negative transition of the PPM output pulse, respectively. The positive edge of the input clock signal is modulated by the first PPM circuit according to input set of data (N1 bits) while the negative edge of the input clock signal is modulated by the second PPM circuit according to input data (N2 bits).

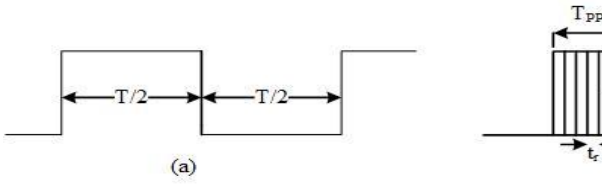

Fig. 4: The eye diagram of the input and the output signals of the PPM circuits. (a) The input clock signal with 50% duty cycle, and (b) The generated data signal from the main clock signal.

Fig. 4 shows the timing diagram of a clock signal with the period of *T* and 50% duty cycle where the rising edge is modulated over the time $T_{PPM-1}$and the falling edge is modulated over the time T_{PPM-2}, respectively. The move in time that occurs to the positive or the negative edge of the input clock signal according to the input data sequence is called the time resolution t_r. Each positive edge can be at one of (2^{N1}) possible positions within the allowed time spacing T_{PPM-1}according to the input data sequence N1. In the same way, each negative edge can be at one of (2^{N2}) possiblepositions within the allowed time spacing T_{PPM-2} according to the input data sequence N2.

For a given binary data sequence which presented in table 1, where B0 is the LSB and BN-1 is the MSB, the delay values are encoded for bit Bi as follows:

$$\text{Edge delay assignment} = 2 \times i \times t_r \times B_i \quad (1)$$

Where i = 0: N-1. If any B value is zero, no delay is assigned.

Table 1. The delay assignment for n bits [12].

B_{N-1}	B_{N-2}	……..	B_2	B_1	B_0	**Total delay assigned to the clock edge**
0	0	……..	0	0	0	0
0	0	……..	0	0	1	t_r
0	0	……..	0	1	0	$2t_r$
0	0	……..	0	1	1	$3t_r$
.		……..	.	.	.	…….
.		……..	.	.	.	…….
1	0	……..	1	0	1	$t_r \times \sum_{i=1}^{N-1}(B_i \times 2^i)$
.	.	……..	.	.	.	…….
1	1	……..	1	0	1	$t_r \times (2^N-3)$
1	1	……..	1	1	0	$t_r \times (2^N-2)$
1	1	……..	1	1	1	$t_r \times (2^N-1)$

Table 1 shows the total amount of the delay assigned to either the rising or falling edge of the input clock signal for N bits input data set (B_0:B_{N-1}) with all probable binary combinations. This hierarchical mapping of delay assignments assures a one-to-one mapping of data codes to delay values. In another meaning, any data code combination always results in an exclusive delay assignment. Consequently, the DPPM architecture is designed ensuring the recovery and the decoding of DPPM signals with the highest possible delay resolution t_r.

Fig. 5 depicts the PPM circuit which is used in the transmitter side and presented in [13]. As illustrated in Fig.5, the number of stages is equal to the number of transmitted bits with the delayed assignment. A reference clock signal is fed to the hierarchical delay structure. Each level has a delay element calculated as described in the following equations:

$$t_r = T_{PPM-1}/2^{N1} \quad \text{, for the positive edge.} \tag{2}$$

And

$$t_r = T_{PPM-2}/2^{N2} \text{,for negative edge.} \tag{3}$$

Where N1and N2 are the number of transmitted bits usingthe positive and the negative edges of the input clock, respectively. TPPM-1 and TPPM-2 can be chosen to be equal, in such a case: N1=N2, hence the total number of transmitted bits is: $N = 2 \times N1 = 2 \times N2$

According to equations (2, 3) the clock edge is shifted according to the input data sequence. When the multiplexed input bits are all 0's, the time difference is zero. Alternatively, the maximum time difference occurs when the input bits are all 1's.

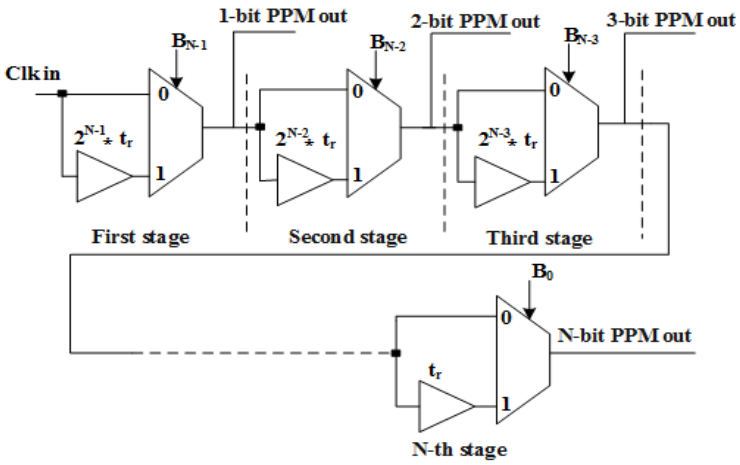

Fig.5. The PPM circuit diagram.

As indicated in Fig.5 the number of stages is equal to the number of transmitted bits with the delay assignment calculated according to equations 2 and 3. The proposed link uses two PPM circuitsone of them to modulate the positive edge of the input clock according to transmitted bits N1 and the other isto modulate the negative edge of the input clock according to transmitted bits N2 and they generate two PPM signals one of them for the modulated positive edge and the other is for the modulated negative edge and they have non-modulated edges as indicated in Fig. 6(c),(d),respectively. To fix the position of the non-modulated edges of each signal, each PPM output signal and it's reference clock (clk out) are fed to an AND gate, as shown in Fig. 3.The output signal from each AND gate are indicated in Fig.6(e),(f), respectively. To combine the output signal of the PPM circuits after extracting the modulated edges using AND gate, an OR gate is deployed as shown in Fig. 3. The output signal from OR gate represents the transmitted signal with both modulated positive and negative edges and shown in Fig. 6(g).Fig. 6 shows the generation of the transmitted signal. Fig. 6 (a), (c), and (e) shows the process of modulating input data on the rising edge of the clock. On the other hand, Fig. 6 (b), (d), and (f) indicates the modulating input data on the falling edge of the clock. Before sending the modulated data, to compensate the channel attenuation, an output stage circuit is applied. This circuit cancels the distortion caused by the channel and improves the transmitted data signal integrity especially in the long transmission.

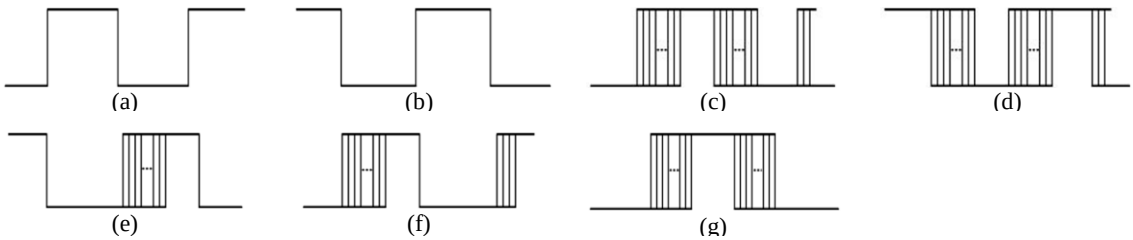

Fig. 6: Transmitted signal generation.(a) The input clock signal, (b) The inverted clock signal, (c) The eye diagram of the PPM_1 output signal,(d) The eye diagram of the PPM_2 output signal, (e) The eye diagram of

the PPM_1 output signal at the end of the AND gate, (f) The eye diagram of the PPM_2 output signal at the end of the AND gate and (g) The eye diagram of the data signal at the end of the OR gate.

B. The receiver circuit

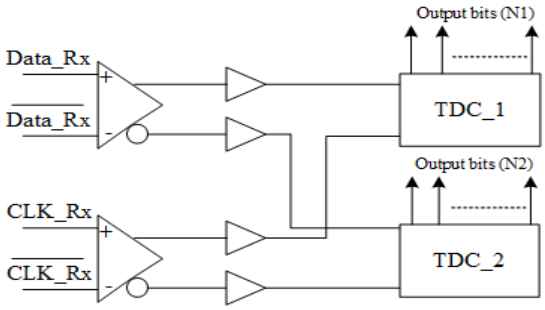

Fig.7.The block diagram of the receiver side of the proposed.

The receiver of the proposed approach shown in Fig.7.The received signal is detected and amplified by a comparator circuit at the first stage of the receiver circuit.Fig.8shows the circuit diagram of the comparator circuit, which consists of six differential amplifier stages. The inputs are terminated in 50Ω because of matching the input resistance of the comparator circuit to the FR-4 channel resistance.

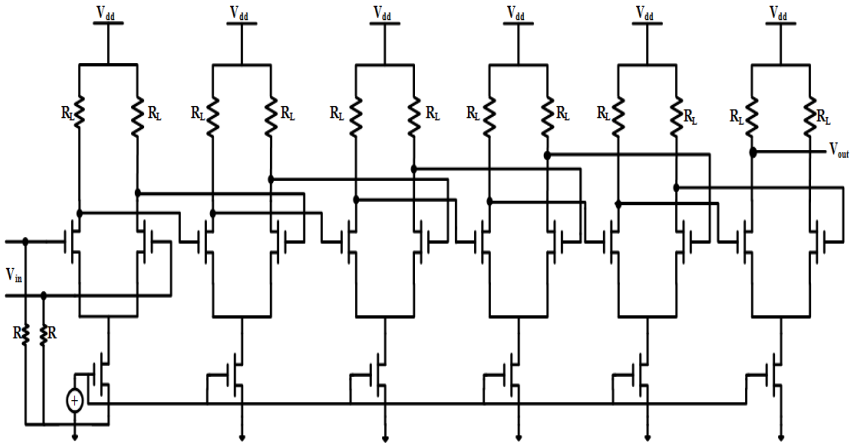

Fig.8. The comparator circuit [12].

The second stage is a TDC circuit which is used to convert the time difference between the rising/falling edges of the data signal and the reference clock into a digital code. Then, the digital code is decoded into a binary sequence which emulates the original data encoded at the transmitter. Two TDC circuits are used in the receiver circuit: TDC_1 converts the time difference between the rising edge of the data signal and the rising edge of the clock pulse signal into a binary code N1 similar to the transmitted code. While TDC_2 converts the time difference between the rising edge of the inverted data signal and the rising edge of the clock pulse signal into a binary code N2 similar to the transmitted code.

A multiplicity of research related to TDC implementation techniques has been executed such as in [14-16]. A fine resolution TDC design is used in the receiver design which is a modified version of a single-cycle-latency circuit explained in [16]and is shown in Fig.10. The TDC implementation is split into two junctures, one of them called signal

propagation and the other called data decoding. The two junctures work in parallel, with the signal-generation lobe processing the encoded data edges whereas the decoder lobe permanently likens the reference clock edge with the processed data signal edges. The selection of the delay values specified to each delay element was prepared to cover all possible delay repetitions but in a hierarchical style. For producing signal transition history before and after all delay elements an XOR gate is applied between various levels in the delay hierarchy. Due to the XOR gate output signal pulse width equals to half of the XOR gate input signal pulse width, a modification has been presented because the data signal pulse width for some codes is not large enough to propagate as the data signal to the XOR gate. This modification is obtained in [16] by employing the data signal as the input data to the D-type flip-flops and employing the clock signal as a trigger clock for the same flip-flops. Using two TDC circuits at the receiver of the proposed link to recover the six transmitted bits using the proposed method, simplifies the circuit design. If we are using only one TDC circuit to recover the six transmitted bits this will make the design suffer from complexity and a lot of power consumption.

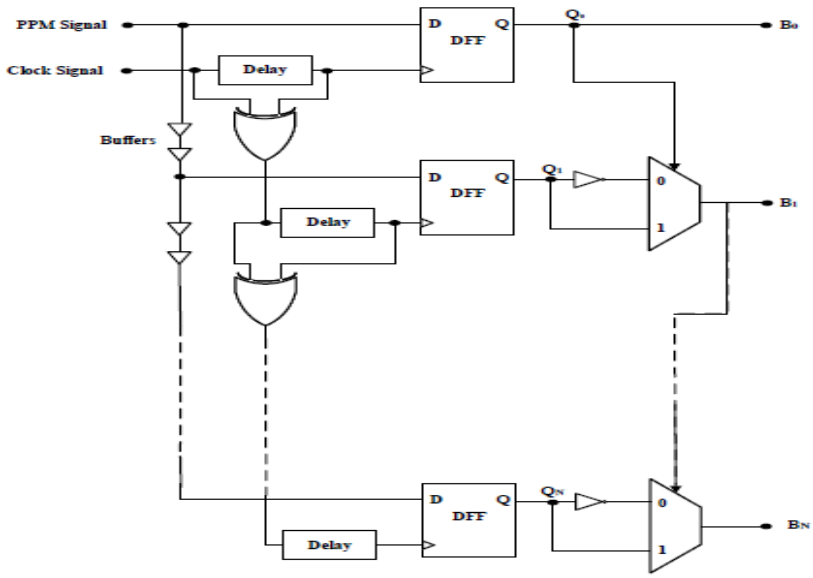

Fig.9.The block diagram of the TDC circuit [16].

III. SIMULATION RESULTS

Using Cadence tools in a mixed signal 130 nm CMOS process, a 6-bit 4.8 Gb/s DMPPM link has been designed and simulated. The DMPPM link utilizes an input clock frequency of 800 MHz. The transmitter and the receiver circuits have been designed using the circuits shown in Fig.3 and 7.

In the 6 bits 4.8 Gb/s link, N1 and N2 have been chosen as: N1 = N2 = N/2 = 3. Hence, the total number of transmitted bits is increased to (N1 + N2) using the same input clock frequency. Since T=1.25 ns, the designed time resolution of the link is then t_r = 45 ps. Fig.10shows the transmitter waveforms. The waveforms are the same as expected as the waveforms illustrated in Fig. 6. It is clear that the rising and the falling edges of the data pulse are spacing equally as designed. Fig.10 (a) and (b) indicate the input and inverted clock signals separately. Fig.10(c) and (d)

illustrate the PPM output signals and indicate that both edges have been modulated in a separate PPM circuit. Fig.10 (e) and (f) indicate the PPM output signal at the end of the AND gate. They illustrate that each signal has one modulated edge and the other edge is not modulated. Fig.10 (g) indicates the OR gate output signal, which illustrates that both the positive edge and the negative edge have been modulated independently and jointed in one signal. Fig.10(g) illustrates that there are 8 positive edge transitions indicating the probable combinations of the 3 input bits represented by N1, which are (000, 001, ……and 111) and 8 negative edge transitions indicating the probable combinations of the 3 input bits represented by N2, which are (000, 001, ……and 111). Hence, the total edge transitions are equal 16 edges. This indicates that the total transmitted bits are increased without complicating the proposed link. The positive or negative transitions are spaced by 45 ps.

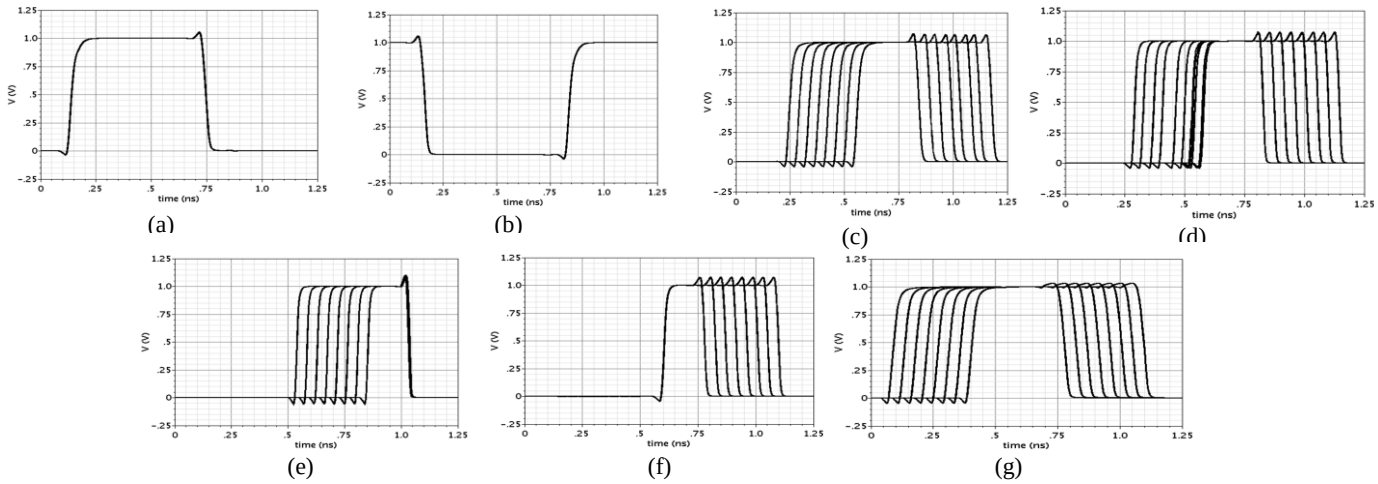

Fig.10. The simulated signals.(a) The input clock signal,(b) The inverted clock signal, (c) The PPM_1 output signal, (d) The PPM _2 output signal, e) The PPM _1 output signal at the end of the AND gate, (f) The PPM _2 output signal at the end of the AND gate and (g) The DMPPM transmitted signal.

Fig.11 shows the received signal at the output of the 20-inch FR4 channel and before the comparator circuit.

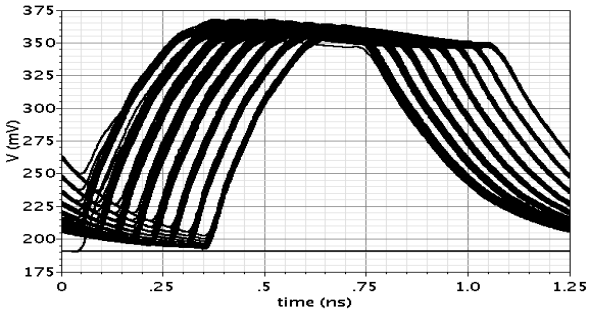

Fig.11.The eye diagram of the received signal at the end of the channel.

While Fig.12 shows the received signal at the output of the comparator circuit. At the end of the comparator circuit, the TDC circuits convert the time difference between signal edges into binary codes.

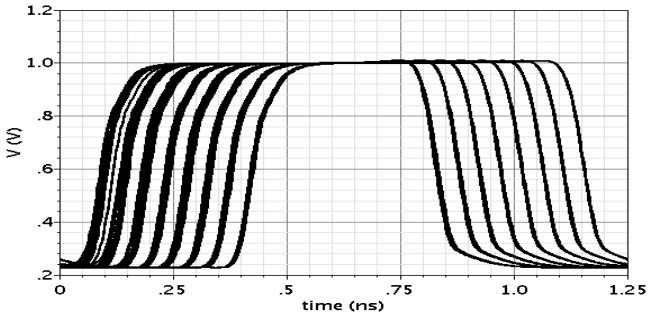

Fig.12.The eye diagram of the received signal at the end of the comparator circuit.

A comparison between the proposed link and a different serial link in terms of the number of transmitted bits, modulation technique, the power consumption, input clock frequency, and the channel length.

Table 2. Comparison table between the designed DMPPM link with other published work.

	This work	**Ref [17] 2008**	**Ref [18] 2016**	**Ref [5] 2013**
Modulation technique	DMPPM	PWAM	PAM-PPM	PAM
Input clock frequency	800MHz	250 MHz	800MHz	2.5GHz
Date rate	4.8 Gb/s	1 Gb/s	4 Gb/s	10 Gb/s
Tx and Rx Power consumption	100mW	131mW	90mW	425mW
Channel Length	30 inch	12 inch	20 inch	27 inch
V_{dd}	1 V	1.2 V	1V	2V/3.5V
CMOS Technology	130 nm\	180 nm	130nm	180 nm

Table 2 shows an accomplishment of the proposed transceiver with other propagated serial data links. The proposed transceiver realizes the highest bit rate over symbol rate. In addition to the input clock frequency signal which used in the proposed transceiver is small. As a result, the transmitted signal occupies lower bandwidth than the other serial data links. Although the Authors in [17] uses smallest input clock frequency signal than in the DMPPM link but the data rate in [17] is very small compared to the data rate in the DMPPM link. Authors in [5] achieve higher bit rate. However, a complex clock recovery system must be used in the receiver because of the non-return to zero nature of transmitted date. This causes an increase in the power consumption. It must be recognized that the number of the serialized bits in the proposed transceiver can be increased without complication.

IV. CONCLUSION

A Dual Modulation pulse position modulation (DMPPM) architecture has been proposed in this paper that increases the total number of transmitted bits without significantly affecting the transmitted signal bandwidth. The proposed architecture modulates both the rising and the falling edges of the input clock signal, which increases the total number of transmitted bits per symbol. The data signal and the clock signal are transmitted over two separate channels. An example of 6-bit 4.8Gb/s DMPPM-TDC link has been designed and simulated in 130nm CMOS using 800MHz as an input clock signal. The simulation results were presented. A comparison between the designed link and other serial links architectures in terms of the number of transmitted bits, the modulation technique, the power consumption, input clock frequency, and the channel length. The proposed link showed an improved performance over other serial links..

References:

[1] P. K. Hanumolu, G.-Y. Wei, and U.-K. Moon, "Equalizers for high-speed serial links," International journal of high speed electronics and systems, vol. 15, pp. 429-458, 2005.

[2] X. Wang and Q. Hu, "Analysis and optimization of combined equalizer for high speed serial link," in Anti-counterfeiting, Security, and Identification (ASID), 2015 IEEE 9th International Conference on, 2015, pp. 43-46.

[3] A. Jain, "Equalization in continuous and discrete time for high speed links using 65 nm technology," 2016.

[4] V. Stojanović, "Channel-limited high-speed links: Modeling, analysis and design," PhD. Thesis, 2004.

[5] B. Song, K. Kim, J. Lee, and J. Burm, "A 0.18-μm CMOS 10-Gb/s Dual-Mode 10-PAM Serial Link Transceiver," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, pp. 457-468, 2013.

[6] W.-H. Chen, G.-K. Dehang, J.-W. Chen, and S.-I. Liu, "A CMOS 400-Mb/s serial link for AS-memory systems using a PWM scheme," IEEE Journal of Solid-State Circuits, vol. 36, pp. 1498-1505, 2001.

[7] N. Ghaderi, Z. D. Ghol, and S. R. Fatemi, "A CMOS 7Gb/s, 4-PAM and 4-PWM, serial link transceiver," Analog Integrated Circuits and Signal Processing, vol. 89, pp. 809-823, 2016.

[8] M. Rashdan, A. Yousif, J. Haslett, and B. Maundy, "A new time-based architecture for serial communication links," in Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on, 2009, pp. 531-534.

[9] M. Rashdan, A. Yousif, J. Haslett, and B. Maundy, "Data link design using a time-based approach," in Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on, 2010, pp. 3977-3980.

[10] M. Rashdan, "Dual-time resolution time-based transceiver for low-power serial interfaces," Analog Integrated Circuits and Signal Processing, vol. 92, pp. 81-89, 2017.

[11] W. Bae, C.-S. Yoon, and D.-K. Jeong, "A low-power pulse position modulation transceiver," in Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, 2015, pp. 1614-1617.

[12] M. Rashdan, A. Yousif, J. Haslett, and B. Maundy, "Differential Time Signaling Data-Link Architecture,"

Journal of Signal Processing Systems, vol. 70, pp. 21-37, 2013.

[13] A. Yousif, M. Rashdan, J. Haslett, and B. Maundy, "A low power and high speed PPM design for ultra wideband communications," in Electrical and Computer Engineering, 2008. CCECE 2008. Canadian Conference on, 2008, pp. 001055-001058.

[14] J. Yu, F. F. Dai, and R. C. Jaeger, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13CMOS Technology," IEEE journal of solid-state circuits, vol. 45, pp. 830-842, 2010.

[15] M. Zanuso, P. Madoglio, S. Levantino, C. Samori, and A. L. Lacaita, "Time-to-digital converter for frequency synthesis based on a digital bang-bang DLL," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, pp. 548-555, 2010.

[16] A. Yousif and J. W. Haslett, "A Fine Resolution TDC Architecture For Next Generation Pet Imaging," IEEE Transactions on Nuclear Science, vol. 54, pp. 1574–1582, October 2007.

[17] C.-Y. Yang and Y. Lee, "A PWM and PAM signaling hybrid technology for serial-link transceivers," IEEE Transactions on Instrumentation and Measurement, vol. 57, pp. 1058-1070, 2008.

[18] W. Madany, M. Rashdan, and E.-S. Hasaneen, "Pulse-position and pulse-amplitude modulation interface for serial data link applications," in Electronics, Communications and Computers (JEC-ECC), 2016 Fourth International Japan-Egypt Conference on, 2016, pp. 95-98.

الملخص العربى

يتم تقديم بنية وصلة بيانات تسلسلية تستند إلى الوقت (DMPPM). في النهج المقترح ، يتم تعديل كل من الحواف الصاعدة والحادة لإشارة مدار الساعة بشكل مستقل. ويسمح استخدام النهج المقترح بزيادة العدد الكلي للبتات المرسلة دون التأثير بشكل كبير على عرض نطاق الإشارة المعدل. تم تصميم نموذج تصميم وصلة DMPPM بسرعة 4.8 بت / ث باستخدام تقنية CMOS بدقة 130 نانومتر. تم استخدام 800 ميجا هرتز كإشارة على مدار الساعة المدخلات. يتم عرض نتائج البحث والمقارنة بين الوصلة المقترحة والروابط التسلسلية الأخرى. اجمالى استهلاك الطاقة بالوصلة أقل من 100mw.