APPLYING THE DERIVATIVE SUPER POSITION METHOD FOR A HIGH LINEAR COMMON SOURCE CMOS POWER AMPLIFIER IN ULTRA-WIDEBAND APPLICATIONS

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ABSTRACT

The problem with the power amplifiers is that raising the gain and output power may affect the other amplifier factors specially in the frequency ultra-band. This paper presents a CMOS power amplifier (PA) for Ultra-Wideband (UWB) applications in 2.2 to 5 GHz using two stages of common source topology with derivative superposition (DS) method. Simulation results show an average power gain of 27.2 dB with an input 1dB compression point (1dB-CP) of -14.6 dBm at 3.2 GHz and an output 1dB compression point (1dB-CP) 12.9 dBm. With an input power of 83.8 mW, from a 1.8 V supply, power added efficiency (PAE) is 47.5% at 3.2 GHz with 50Ω load impedance and stability factor is 7.2 at 3.2GHz. The proposed design has been simulated using TSMC 0.18μm technology. The important parameters that define an RF Power Amplifier are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency, Ruggedness. The design results showed high power output without affecting the other amplifier factors. A comparison with the previous research has been done and the comparison is clearly in favor of the present design.

Keywords: *Ultra-Wideband (UWB), Power amplifier (PA), Derivative Superposition (DS) Method*, Common Source Power Amplifier.

1. INTRODUCTION:

The goal of this research is to design Power Amplifier in an integrated circuit. It is focused on RF Power Amplifier design in 2.2 to 5 GHz frequency band which is suitable for using for Ultra-Wideband (UWB) wireless communication system, In order to keep pace new competitive communication technology.

Many of today's communication devices, especially mobile devices, require high performance, low power consumption ICs to insure steady connectivity and longer battery life. The development of digital devices goes from small to smaller, which needs minimizing the sizes of ICs as possible. One of the best ways to meet this is by fully integrating the communication circuit in one single chip. This would lead to smaller size, lower power consuming and greater performance. The Radio Frequency (RF) power amplifier (PA) is a type of electronic amplifier used to convert a low-power radio-frequency signal into a larger signal of significant power, typically for driving the antenna of a transmitter.

The RF power amplifier plays an important role in RF systems. It is used as a final stage of a transmitter to provide signal power to a transmitting antenna. The basic techniques for RF power amplification can use classes as A, B, C, D, E, and F. The RF Output Power can range from a few mW to MW, depending on applications. Most important parameters that define an RF Power Amplifier are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency, Ruggedness. The values of these parameters are high or low depending on

the applications that uses the RF-PA such as ultra-wideband (UWB) [1]. Figure 1 presents the block diagram of the general RF transceiver. The problem with the power amplifiers is that raising the gain and output power may affect the other amplifier factors specially in the frequency ultra-band.

This paper introduces the design and simulation of common source wide band power amplifier. Also, it presents and simulates the Common Source Power Amplifier with derivative superposition (CS PA with DS) design method. The present design is done in the band (2.2 – 5.0) GHz. Most important parameters that define an RF Power Amplifier are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency, Ruggedness. This paper presents these factors as well as the different classes of power amplifier. The present design results showed high power output without affecting the other amplifier factors. A comparison with the previous research has been done and it shows that the paper results are much better than the results of these research works. The paper has 6 sections. Section (1) is an introduction and section (2) depicts some of the literature review about the topic and section (3) illustrates the simulation of the RF-PA including the common source power amplifier and the common source power amplifier with derivative superposition (CS PA with DS) design method. Section (4) presents the simulation results for both the cases. Section (5) givesa comparison with the previous work, andsection (6) gives some conclusions.A list of the used references is given at the end of the paper.
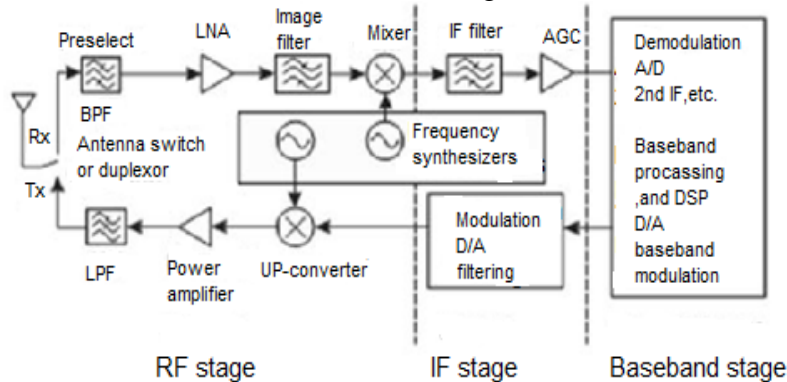

Fig.1. Block diagram of the general RF transceiver[2]

2. A LITERATURE REVIEW

Many topologies have been used in the implementation of these UWB power amplifiers. These topologies include the common source (CS) inductive degeneration, the derivative superposition [3] and the cascaded common source (CS) structure [4]. Normally, the design requirements of the amplifier such as bandwidth, gain, PAE and linearity basically determine the most suitable configurations. In this section, a brief summary of the properties of these topologies is given.

Yileiet. al. offered two-stage of derivative superposition get high gain and good linearity but poor power added efficiency.[3]. Wong et. al. offered a two-stage cascaded common source to get higher gain, good wide bandwidth, good linearity and low power consumption but poor power added efficiency.[4]. Alegre offered common source power amplifier to get high gain and good linearity but poor power added efficiency.[5]. Vu et. al. offered two-stage cascade common source power amplifier to get high gain and high linearity but poor power added efficiency.[6]. Mosalam offered two-stage cascade common source power amplifier to get good gain and good linearity but poor power added efficiency[7].

3.RADIO FREQUENCY POWER AMPLIFIER (RF-PA)
3.1. Design and Analysis of Common Source Power Amplifier:

The design of the CS PA is done in two stages: the first stage consists of two transistors connected as cascode common source and a

biasing circuit. The RF signal input to the first stage with V_{DD} and the output of the first stage is the input of the second stage. The second stage consists of one transistor connected as simple

common source and biasing circuit. The input of the second stage is the output of the first stage with V_{DD}. We get the total output signal from the second stage
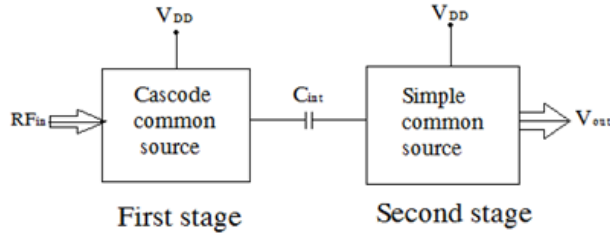

Fig.2. of the two- The block diagram stage UWB CS PA

The first stage consists of a current mirror for biasing (MC1) and a cascade common source to get high gain. The biasing circuit is a current mirror with the width is about 6µm. Elements R1, R2, Ls1 are used for linearity and stability. About "180pH" Lg1 is needed forimpedance matching and about "180pH" Ld1 is used as a shunt peaking inductor. C1, C2, C3 are usedfor RF shunting. The main transistor M1 in the first stage amplifies the signal. To calculate the size of the transistor M1, the following equation is used:

$$I_{DD} = 0.5\mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_t)^2 \qquad (1)$$

where $V_{GS1} = 0.8V$, $V_t = 0.5V$, $\mu_n = 0.03903 \ m^2/V-s$, and $C_{ox} = 0.00946 \ F/m^2$, for a typical $0.18\mu m$ silicon CMOS process. The requisite trans-conductance (g_{m1})can be additionally determinedby the next equation [8]:

$$g_{m1} = \frac{\partial I_{DD}}{\partial V_{GS}} = 2 \left[\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \right] (V_{GS1} - V_t) \qquad (2)$$

Reorganizing (1) to be $(V_{GS1} - V_t) = \sqrt{I_{DD} / \left[0.5\mu_n C_{ox} \frac{W}{L} \right]}$ and replacing it into

equation (2), the equation for g_{m1} can be simplified to:

$$g_{m1} = 2\sqrt{0.5\mu_n C_{ox} \frac{W}{L} I_{DD}} = \sqrt{\beta . I_{DD}} \qquad (3)$$

where$\beta = 0.5\mu_n C_{ox} \frac{W}{L}$ is well-known as trans-conductance parameter. The width of M1 is found to be about 184 µm and the width of Mb is found to be about 80 µm.

The second stage consists of a current mirror for biasing and a simple common source without cascade to get high gain as shown in figure 3. This PA gives a total dc power of 77.22mW from a 1.8V dc supply and total drain current of about 42.9mA. This stage has a biasing circuit of MC2 current mirror with a width of about "6µm". The elements R3, R4,Ls2 are used for linearity and stability enhance. About "180pH" Ld2 is used as a shunt peaking inductor. C4, C5 are used to RF shunting, and M2 is the main transistor in second stage that amplifies the signal using equations (1-3) to determine the width of about 184µm. The elements Cin,Cint,Cout are used for dc blocking. Cadence software has been used to design the circuit and make the simulation.
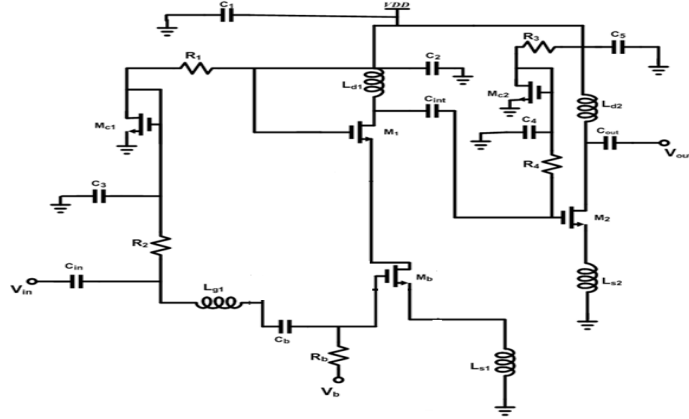
Fig.3. The circuit diagram of the two-stage CS PA

The equivalent circuit of the two stage CS PA, with neglecting the biasing circuit, (the biasing circuit in the first stage consists of (M_{C1} current mirror ,R_1, R_2, R_b, andC_b), neglecting C_1, C_2,C_3, used for shunting RF. The biasing circuit in the second stage consists of (M_{C2} current mirror, R_3, and R_4), neglecting L_{g1}, L_{s1}, L_{d1}, L_{s2}, L_{d2} as with very small resistant and neglecting C_4, C_5, used for shunting RF. Figure (4) shows the equivalent circuit of the first stage of CS PA.
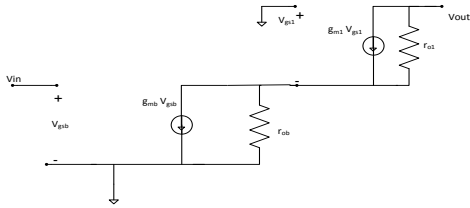
Fig.4. Equivalent circuit of the first stage of CS PA

$$V_{in} = V_{gsb} \tag{4}$$

$$V_{out} = -(r_{ob} + r_{o1})V_{gs1}g_{m1} \tag{5}$$

$$V_{gs1}g_{m1} = V_{gsb}g_{mb} \tag{6}$$

$$-V_{gs1} = V_{gsb} = V_{in}$$
$$A_{V1} = \frac{V_{out}}{V_{in}} = \frac{-(r_{ob} + r_{o1})V_{gs1}g_{m1}}{V_{in}}$$
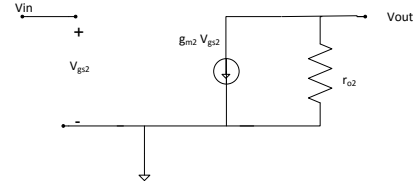$$A_{V1} = (r_{ob} + r_{o1})g_{m1} \tag{7}$$

Fig.5. Equivalent circuit of the second stage of CS PA

$$V_{in} = V_{gs2} \tag{8}$$

$$V_{out} = -V_{gs2}g_{m2}r_{o2} \tag{9}$$

$$A_{V2} = \frac{V_{out}}{V_{in}} = \frac{-V_{gs2}g_{m2}r_{o2}}{V_{in}} = -g_{m2}r_{o2} \tag{10}$$

$$A_{VT} = A_{V1} * A_{V2}$$
$$= (r_{ob} + r_{o1})g_{m1} * (-g_{m2}r_{o2})$$
$$=-(r_{ob} + r_{o1})g_{m1}g_{m2}r_{o2} \tag{11}$$

3.2. The Common Source Power Amplifier with Derivative Superposition (CS PA with DS):
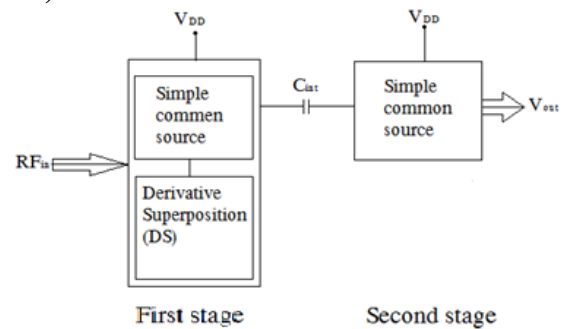

Fig.6. The block diagram of the two-stage UWB PA with DS

The design of the UWB PA with DS is done in two stages, the first stage consists of the derivative superpositioncascode with simple common source and a biasing circuit, the RF signal input to the first stage with V_{DD}.The output of the first stage is the input of the second stage. The second stage consists of one transistor connected as a simple common source and a biasing circuit. The input of the second stage is the output of the first stage with V_{DD}. We get the total output signal from the second stage.

The first stage consists of current mirror for biasing, common source to get high gain and derivative superposition method to get high linearity. Second stage consists of current mirror for biasing and simple common source to get the high gain as shown infigure 7. This PA gives total dc power 83.8mW from a 1.8V dc supply and total drain current of about 46.6mA.

The first stage consists of biasing circuit (MC1 current mirror "width is about 6μm", R1, R2, Ls1 "used for linearity and stability advance, it is about 180pH", Lg1 (needed toimpedance matching, it is about 180pH", Ld1 (used as a shunt peaking inductor", C1, C2, C3 (used for RF shunting", M1 (the main transistor in the first stage that amplify the signal). To calculate the size of transistor M1 the following equation is used:

$$I_{DD} = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_t)^2 \qquad (12)$$

where $V_{GS1} = 0.8V$, $V_t = 0.5V$, $\mu_n = 0.03903 \ m^2/V-s$, and $C_{ox} = 0.00946 \ F/m^2$,

for a typical -0.18 μm silicon CMOS process.The requisite trans-conductance (g_{m1})can be additionally determinedby the next equation [8]:

$$g_{m1} = \frac{\partial I_{DD}}{\partial V_{GS}} = 2\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right](V_{GS1} - V_t) \qquad (13)$$

Reorganization (12) to $(V_{GS1} - V_t) = \sqrt{I_{DD}/\left[0.5\mu_n C_{ox}\frac{W}{L}\right]}$ and replacing into (13), the equation for g_{m1}can be simplified to:

$$g_{m1} = 2\sqrt{0.5\mu_n C_{ox}\frac{W}{L}I_{DD}} = \sqrt{\beta.I_{DD}} \qquad (14)$$

where$\beta = 0.5\mu_n C_{ox}\frac{W}{L}$ is well-known as trans-conductance parameter.

The width of M1 is determined as about 184 μm. At finally, the first stage containing the derivative superposition consists of two parallel transistors (Ma and Mb) and a biasing circuit (Ra, Rb, Ca, Cb, Va and Vb). Va is the voltage that biases Ma in sub-threshold and Vb is the voltage that biases Mb in a strong inversion region [9].

The second stage consists of a biasing circuit (MC2 current mirror "width is about 6μm", R3, R4, Ls2 "used for linearity and stability enhance, it is about 180pH", Ld2 "used as a shunt peaking inductor", C4, C5 "used for RF shunting", and M2 "the main transistor in second stage that amplifies the signal using equations (12-14) to determine the width as about 184μm"). Cin, Cint,Cout are used for dc blocking.
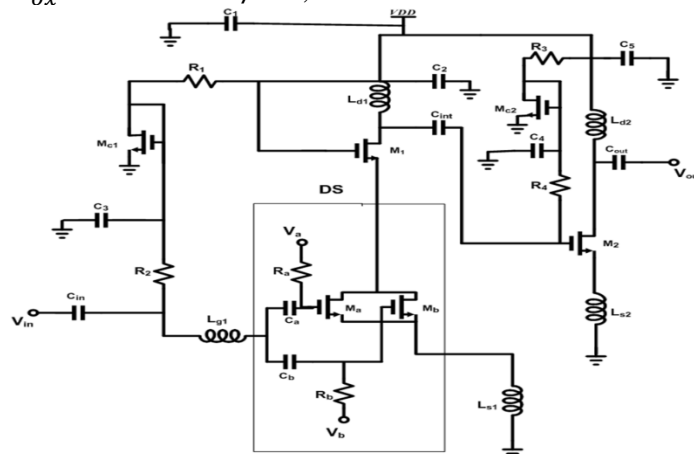

Fig.7. The circuit diagram of the two-stage CS PA with DS

The equivalent circuit of the two stage UWB PA with DS , with neglecting the biasing circuit , (the biasing circuit in the first stage is consist of (M_{C1} current mirror ,R_1, R_2,R_a, R_b, C_a, andC_b)), neglecting C_1, C_2,C_3, as used to shunting RF . (The biasing circuit in the second stage is consist of (M_{C2} current mirror, R_3, and R_4), neglecting C_4, C_5, as used to shunting RF and neglecting L_{g1}, L_{s1}, L_{d1}, L_{d2}, L_{s2}, as with very small resistant.Figure (8) shows the equivalent circuit of the first stage of UWB PA with DS.
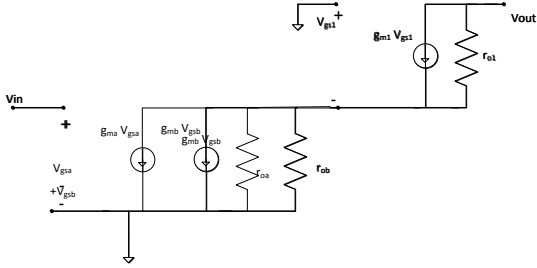
Fig.8. the equivalent circuit of the first stage of UWB PA with DS

$$V_{in} = V_{gsa} + V_{gsb} \qquad (15)$$

$$= -(V_{gsa}g_{ma} + V_{gsb}g_{mb})(r_{oa}//r_{ob})$$
$$V_{out} = -V_{gs2}g_{m2}r_{o2}$$
$$V_{gs2}g_{m2} = V_{gsa}g_{ma} + V_{gsb}g_{mb}$$
$$A_{V1} = \frac{V_{out}}{V_{in}}$$
$$= \frac{-V_{gs2}g_{m2}r_{o2}}{-(V_{gsa}g_{ma} + V_{gsb}g_{mb})(r_{oa}//r_{ob})}$$
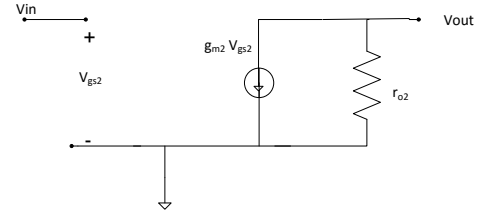$$A_{V1} = \frac{r_{o2}}{(r_{oa}//r_{ob})}$$
$$(16)$$

Fig.9. the equivalent circuit of the second stage of UWB PA with DS

$$V_{in} = V_{gs2} \qquad (17)$$

$$V_{out} = -V_{gs2}g_{m2}r_{o2} \qquad (18)$$
$$A_{V2} = \frac{V_{out}}{V_{in}} = \frac{-V_{gs2}g_{m2}r_{o2}}{V_{in}} = -g_{m2}r_{o2} \quad (19)$$
$$A_{VT} = A_{V1} * A_{V2}$$
$$= \frac{r_{o2}}{(r_{oa}//r_{ob})} * (-g_{m2}r_{o2}) = -\frac{r_{o2}{}^2 g_{m2}}{(r_{oa}//r_{ob})} \qquad (20)$$

4. Simulation results:
4.1. Simulation results for CS PA:
4.1.1. S parameters:

The PA is designed using TSMC 0.18μm technology. The simulation is achieved using Cadence and based on the device models provided by this technology. This PA operates at 2.2 to 5GHz under 1.8V voltage supply. Figure 10 shows the scattering functions S11, S21, S12, and S22. Table 1 shows the value of scattering functions S11, S21, S12, and S22 at 3.2 GHz.

Table 1 the value of scattering functions at 3.2 GHz

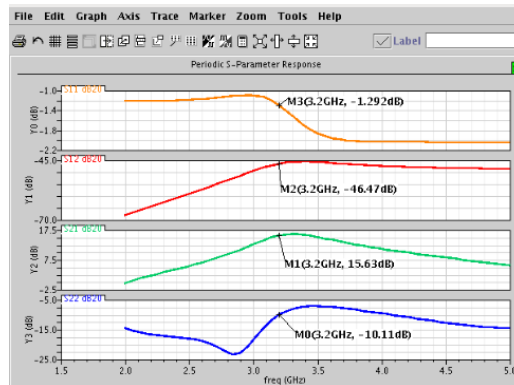| Function	Frequency	Value
S11	3.2 GHz	-1.3 dB
S12	3.2 GHz	-46.5 dB
S21	3.2 GHz	15.5 dB
S22	3.2 GHz	-10.3 dB

Fig.10. the scattering functions S11, S21, S12, and S22

4.1.2. Stability analysis of the CS PA:

The S-parameter simulation is used to measure stability of the transistor by the stability

factor (KF) where its value should be more than one. Figure 11 shows a good value of the stability factor (KF) is about 3.8 at 3.2GHz.
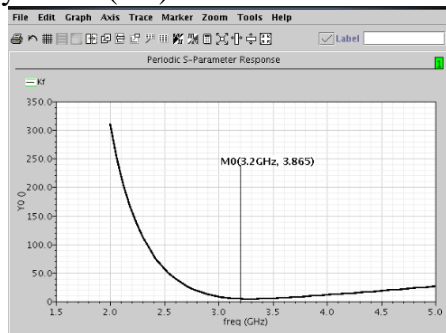

Fig.11. Values of the stability factor (KF).

Figure 12 illustrates the relation between the power added efficiency (PAE) and the input power at 3.2GHz where the PAE equals 12%, 39.5%, 47%, at -10dBm, -5dBm, 0dBm. These are good values of PAE.
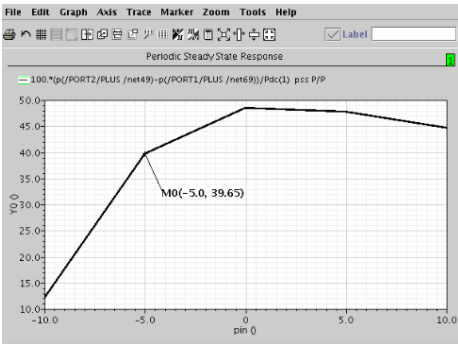

Fig.12. The power added efficiency (PAE) and input power

4.1.3. Linearity of the CS PA:

The linearity is measured with 1dB method shown in figure 13 for the input and in figure 14 for the output. Input Referred 1dB is about -4.7, Output Referred 1dB is about 14 at 3.2GHz.
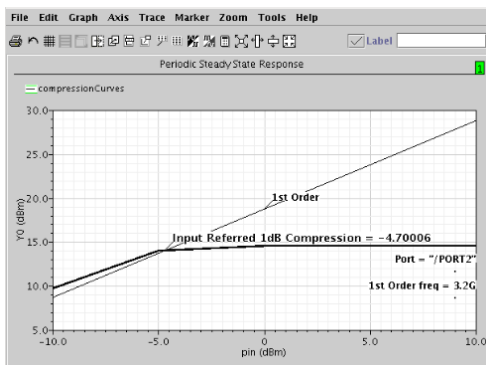

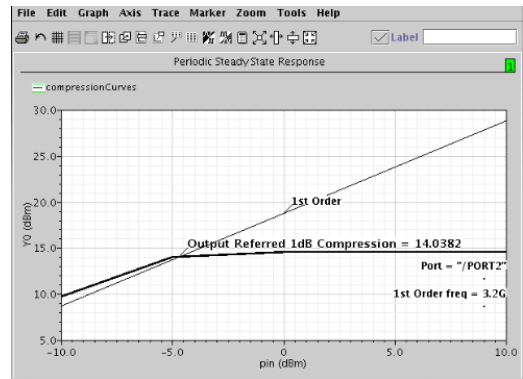**Fig.13**. The Input Referred 1dB and input power

Fig.14. The Output Referred 1dB and input power

4.2. Simulation results for CS PA with DS:
4.2.1 S parameter:

The PA is designed using TSMC 0.18μm technology. The simulation is achieved using Cadence and based on the device models provided by this technology. This PA operates at 2.2 to 5GHz under 1.8V voltage supply. Figure 15 shows the acattering functions S11, S12, S21, S22 respectively. From the figure it is seen that these functions have good values in the given frequency range. Table 2 shows the value of scattering functions at different frequencies.

Table 2. the value of scattering functions at different frequency

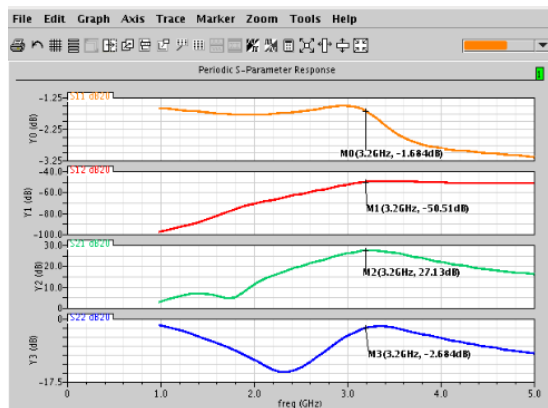| Frequency	S11	S12	S21	S22
2.2 GHz	-1.77 dB	-66.7 dB	15.36 dB	-14.5 dB
3.2 GHz	-1.67 dB	-50.7 dB	27.19 dB	-2.6 dB
4.2 GHz	-2.9 dB	-51.5 dB	20.24 dB	-6.5 dB
5.0 GHz	-3.1 dB	-51.8 dB	16.2 dB	-9.5 dB

Fig.15.the scattering functions S11, S12, S21, and S22

4.2.2. Stability analysis of the CS PA with DS:

The S-parameter simulation is used to measure stability of a transistor by the stability

factor (KF) where its value should be more than one. Figure 16 shows the stability factor (KF) with a very good value of 7.2 at 3.2GHz.
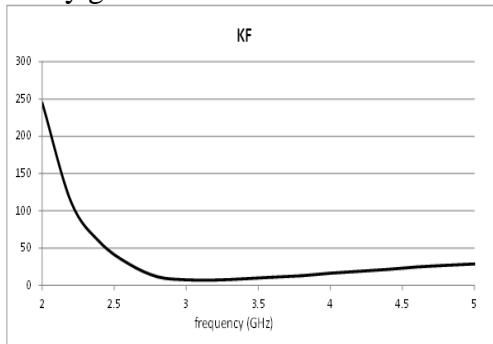

Fig.16. Values of the stability factor (KF).

Figure 17 illustrates the relationship between the power added efficiency (PAE) and the input power at 3.2GHz where the PAE equals 43.5%, 47.5%, 48%, at -10dBm, -5dBm, 0dBm. This shows good values to the PAE.
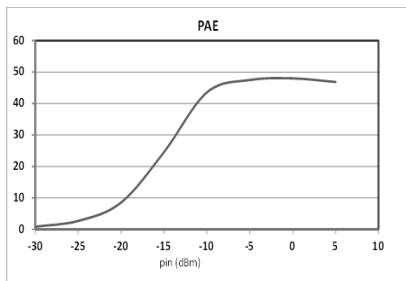

Fig.17. The Power added efficiency (PAE) and input power

Figure 18 illustrates the relationship between the power added efficiency (PAE) and input frequency at input power -5dBm where the PAE equals 40%, 46%, 47.5%,46.5% at 2.6GHz, 3GHz, 3.2GHz, 3.6GHz. This shows very good values to the PAE.
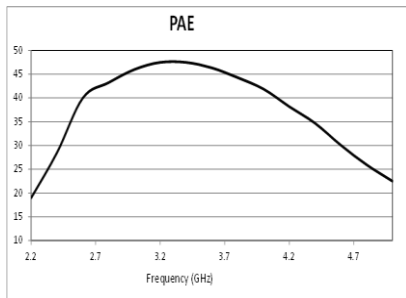

Fig.18. The Power added efficiency (PAE) and input frequency

4.2.3. Linearity of the CS PA:

The linearity is measured with 1dB method shown in figure 19. The Input Referred 1dB is about -14.6 and the Output Referred 1dB

is about 12.9 at 3.2GHz. Figure 20 and figure 21 show the Input Referred 1 dB and the Output Referred 1 dB respectively. Notice that in figure 20, The Input Referred 1dB at input power -5dBm and the Output Referred 1 dB at
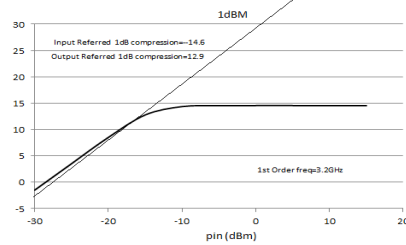

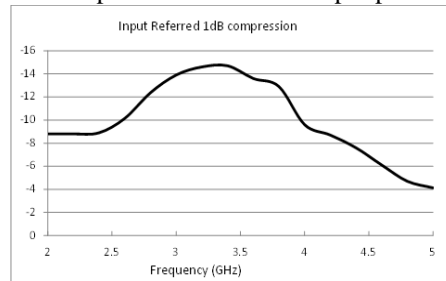**Fig.19.** The Input Referred 1dB at input power -5dBm

Fig. 20. The Input Referred 1dB compression and frequency
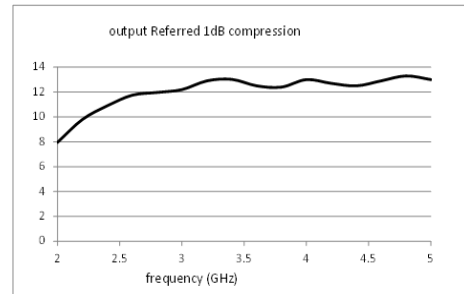

Fig.21. The Output Referred 1dB compression and frequency

5. A Comparison of Simulation Results with the Previous Literature Work

In this paper, we present two different designs of two stages UWB PA with different performance. The simulation results of PA discussed in section 4.1, 4.2 have the best performance in terms of the 3 dB bandwidth, matching, and power added efficiency, linearity and output power. Table (3) shows the performance summary of the two UWB PAs in comparison to the recently published UWB PA.In the second design the simulation result is greater the simulation result for the first design as using Derivative Supposition Method , that lead to high gain ,high linearity, and high power adding efficiency.

6. CONCLUSIONS

Two designs of power amplifier have been introduced. In the First design, a $0.18\mu m$ CMOS UWB PA for lower band UWB system (2.2 to 5GHz) is simulated. By using a two-stage CS, the simulated PA achieved a 15.63 dB gain and up to a maximum of 39.6% power added efficiency at 3.2 GHz using a 50 Ω load termination, while consuming only 77.3 mW. Input Referred 1dB compression=-4.7dBm, Output Referred 1dB compression=14.03dBm.

In the second design, A $0.18\mu m$ CMOS UWB PA for lower band UWB system (2.2 to 5GHz) is simulated. By using a two-stage CS and Derivative Supposition Method, the proposed PA achieved a 27.19 dB gain and up to a maximum of 47.5% power efficiency at 3.2 GHz using a 50 Ω load termination, while consuming only 83.8mW. Input Referred 1dB compression=-12.9, Output Referred 1dB compression=14.6.

Table 3: Relationship of UWB CMOS PA performances available and the present work

Ref.		3dB BW (GHz)	S_{11} (dB)	S_{22}(dB)	Gain (dB)	P_{1dB} (dBm)	PAE %	Power (mW)
[7]		3 to7	<-5	<-4	13 ± 1	+5(output)	13%	21
[5]		2 to 3	N/A	N/A	$15.8 \pm .0.1$	+20.03(output)	22%	N/A
[6]		2.4 to 2.48	<-18	<-15	37.7	−24.5 (input)	24.5%	N/A
[10]		2.9 to5.2	<-5.7	<-5.5	22.3	−11.5 (input) +9.8(output)	26%	25
[11]		3 to7	<-5	<-7	10	>0 (output)	12%	15
Ourcircuits	1	2.2to 5	<-1.29	<-10.11	15.6	−4.5 (input) +14.5 (output)	39.6%	77.3
	2	2.2 to 5	<-1.67	<-2.6	27.19	−12.9 (input) +14.6 (output)	47.5%	83.8

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